Review on Performance of different Low Power SRAM Cell Structures

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ABSTRACT
Scaling in Silicon technology, usage of SRAM Cells has been increased to large extent while designing the embedded Cache and system on-chips in CMOS technology. Power consumption, packing density and the speed are the major factors of concern for designing a chip. The consumption of power and speed of SRAMs are some important issues among a number of factors that provides a solution which describes multiple designs that minimize the consumption of power and this review article is also based on that. This article presents the simulation of 6T, 9T, LP10T, ST10T and WRE8T SRAM cells. All the simulations have been carried out on 90nm at Microwind EDA tool.

General Terms
Low Power VLSI design

Keywords
Cache Memory, CMOS, Hold Power, Speed.

1. INTRODUCTION
THE demand of battery operated high speed portable devices like notebook, laptop computers, personal digital assistants, cellular phones, etc. increase day by day. High speed portable devices require primary memory that responds faster. For that purpose, static random access memory (SRAM) is used, which is faster and refreshing is not needed again and again. Dynamic power dissipation and leakage current are the main issues of high speed SRAM cells because this unwanted power dissipation reduces the battery backup life of portable devices. So it is required to have a SRAM cell design, having both low static and dynamic power dissipations.

Supply voltage is scaled to maintain the power consumption within limit. However, scaling of supply voltage is limited by the high performance requirement. Hence, the scaling of supply voltage only may not be sufficient to maintain the power density within limit, which is required for power sensitive applications. Circuit techniques and system level techniques are also required along with supply voltage scaling to achieve low power designs [1].

Aggressive scaling of the devices not only increases the subthreshold leakage but also has other negative impacts such as increased drain induced barrier lowering (DIBL), threshold voltage roll off, reduced on current to off current ratio, and increased source to drain resistance [2]. V_{th} roll off increases the dependence of V_{th} on the channel length. A small variation in channel length might result in large threshold voltage variation, which makes device characteristics unpredictable. To avoid these short channel effects, oxide thickness scaling and higher and non uniform doping need to be incorporated [3] as the devices are scaled. The low oxide thickness gives rise to a high electric field, resulting in considerable direct tunnelling current [4]. Higher doping results in a high electric field across the reverse biased p–n junctions (source-substrate or drain substrate) which cause significant band to band tunnelling of electrons from the valence band of the p region to the conduction band of the n region. Peak halo doping (P+) is restricted such that the BTBT component is maintained reasonably small compared to the other leakage components. In another technique [5], a low area overhead adaptive body bias circuit is proposed to compensate for aging and process variations to improve the SRAM reliability and yield. The p ABB circuit consists of a threshold voltage sensing circuit and an on chip analog controller for power reduction. A multi threshold complementary metal oxide semiconductor technology provides low leakage and high performance operation by utilizing high speed, low threshold voltage transistors during active mode and low leakage, high threshold voltage transistors during sleep mode, which reduces the static power dissipation of the SRAM circuit [6,7].

For scaled VLSI devices, subthreshold leakage current, junction leakage current and gate leakage current are becoming important leakage component, for applications such as embedded cache and battery operated systems where leakage currents must be kept extremely low. Therefore, leakage is a serious issue in scaled technology.

An on/off current ratio is often used as a gauge for this issue, where the on-current refers to the cell current drawn by an accessed cell during the read operation from the sensing bitline while the off-current refers to the leakage current drawn by all the other unaccessed cells from the other complementary bitline on the same column. Typically, a rule of thumb demands that this on/off ratio is greater than 10 so that there will be adequate voltage swing between the bitline pair at the moment when the sense amplifier is activated to ensure reliable read operation.

In this review paper, low power SRAM cell topologies are studied and simulated. 6T SRAM cell suffer with severe power dissipation. To avoid this problem 9T, LP10T, ST10T and WRE8T was proposed with stack transistor introduced.

The rest of the paper is organized in the following order. Section II presents literature review on existing low power SRAM cells. Result analysis are discussed and compared in Section III. Finally, the concluding remarks are provided in Section IV.

2. LITERATURE REVIEW
This article presents the simulation of 6T, 9T, LP10T, ST10T and WRE8T SRAM cells. All the simulations have been carried out on 90nm at Microwind EDA tool.

2.1 6T SRAM cell
Kim TH, Liu J, Keane J, Kim CH. 2008 proposes 6T. Fig. 1 shows the circuit diagram of a conventional SRAM cell [8]. Before the read operation begins, the bit line (BL) and bitbar line (BLB) are precharged to as high as supply voltage Vdd.

When the word line (WL) is selected, the access transistors are turned on. This will cause a current to flow from supply voltage (Vdd) through the pull up transistor TP1 of the node storing ‘‘1’’. On the other side, current will flow from the precharged bitbar line to ground, thus discharging bitbar line. Thus, a differential voltage develops between the BL and BL. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output.

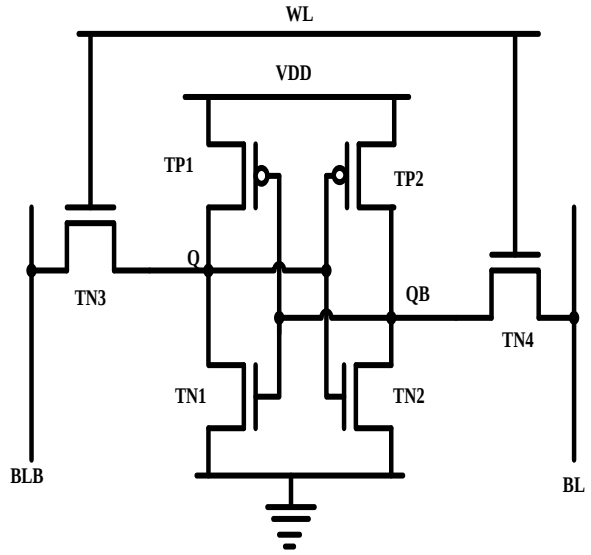

Fig 1: Conventional 6T SRAM cell[8]

2.2 9T SRAM cell

Liu Z and Kursun V. 2008 introduce 9T SRAM [9] is shown in Fig.2. Write occurs just as in the 6T SRAM cell. Reading occurs separately through N5, N6 and N7 controlled by the read signal (RWL) going high. This design has the problem of the high bit line capacitance with more pass transistors on the bit line.

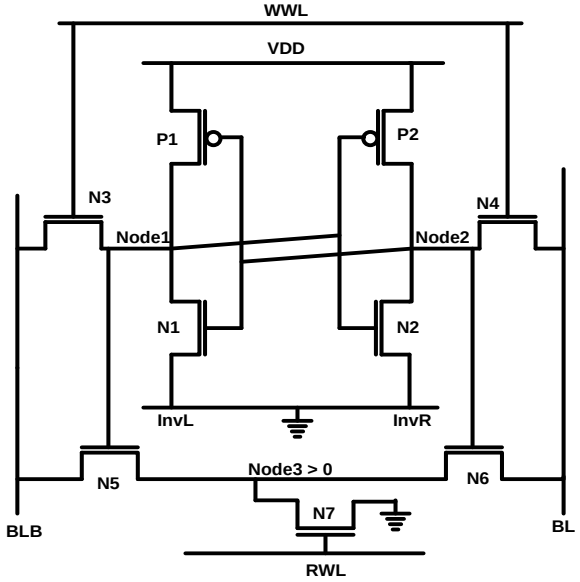

Fig 2: 9T SRAM Cell[9]

2.3 Fully Differential Low Power 10T SRAM

Singh S, Arora N, Gupta N, Suthar M. 2012 proposes the fully differential low power 10T SRAM [10] bit cell is shown in Fig.3. The design strategy of cell is the series connection of a tail transistor. The gate electrode of this device is controlled by the output of an XOR gate, inputs of which are tapped from write word line (WWL) and read word line (RWL) control signals coming from the WWL and the RWL drivers. The XOR gate and the tail transistor are shared by all the cells in a row. The tail transistor has to be appropriately up sized for sinking currents from all the cells in the row. Without this read buffer, a cell with such small drivers and series connected tail transistor would exhibit unacceptably low read static noise margin (RSNM), resulting in read instability.

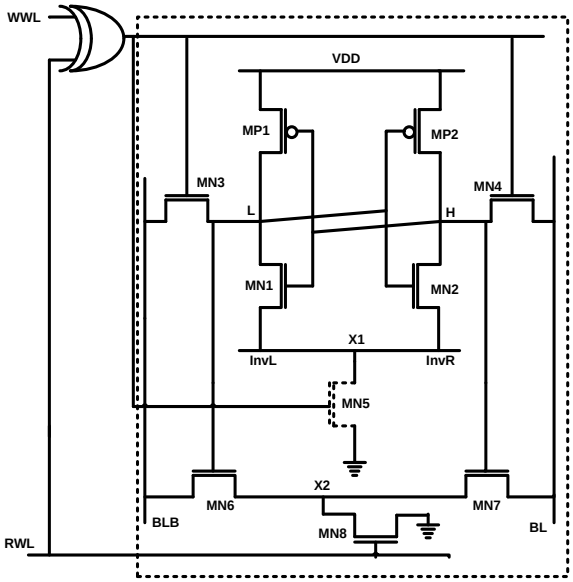

Fig 3: Fully Differential Low Power 10T SRAM (LP10T)[10]

2.4 Schmitt trigger based 10T SRAM cell (ST10T)

J. P. Kulkarni, K. Kim, and K. Roy, 2007 designed the Schmitt trigger based 10T SRAM cell [11] is shown in Fig.4. Extra devices MN5/6/7/8 of ST10T are of minimum width. This extra transistor makes read faster than LP10T.

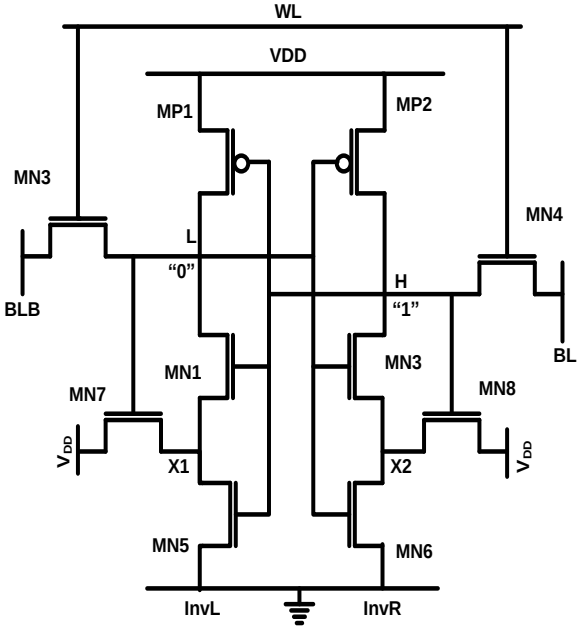

Fig 4: Schmitt trigger based 10T SRAM cell (ST10T)[11]

2.5 write-and-read-enhanced 8T SRAM cell (WRE8T)

Ghasem Pasandi and Sied Mehdi Fakhraie 2014 proposed the 8T SRAM cell. Fig. 5 shows circuit diagram of 8T SRAM cell[12]. In this cell, M5 is write access transistor and M6 is for read access. Having individual access transistors in our cell, it is possible to increase size of write access transistor to improve write-ability and choose minimum size for read access transistor to enhance read stability, whereas in 6T there is a conflict while sizing the access transistors. In the proposed SRAM cell, the added pMOS and nMOS transistors (M7, M8) become OFF during write operation. This interrupts VDD and GND connections of the left inverter in the cell. Thus, left inverter becomes weaker during write operation, and a relatively stronger write access transistor can easily write the input to our cell.

In WRE8T, before read operation bit-line of read (BLT) is precharged to VDD, and then by asserting RWL signal, M6 (Fig. 5) becomes ON and according to the stored data at node q, the capacitance of BLT bit-line is discharged or remains unchanged.

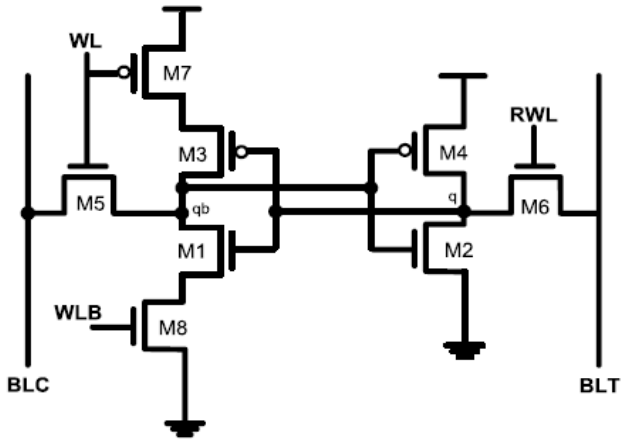

Fig 5: Write-And-Read-Enhanced 8T SRAM cell (WRE8T)[12].

3. RESULT ANALYSIS

All the circuits have been simulated using 90 nm technology on MicroWind tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns.

3.1 Leakage Power

Fig. 6 shows comparision of leakage power dissipation.The standby leakage in embedded cache is an alarming issue in deep-submicrometer technology. The leakage current is one of the major contributors to the total power dissipation in an SRAM cell because a major part of the cache remains idle most of the time except for the row being accessed. The total leakage current in an SRAM cell mainly (ignoring other minor leakage components such as *I*GIDL and *I*punchthrough) consists of the subthreshold leakage current (*I*sub), the gate leakage current (*Ig*), and the BTBT (band-to-band tunneling) or junction leakage current (*I*JN) through different devices. It is observed that LP10T consume lowest power.

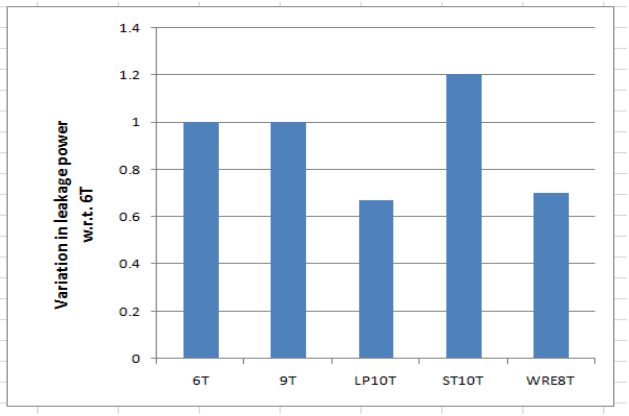

Fig 6: comparison of leakage power dissipation

3.2 Read Access Time(RAT)

Fig. 7 shows comparision of read access time. *T*RA (read access time or read delay) is estimated from the time when RWL (WL) (wordline) is activated to the time when bitline (BL)/bitline bar(BLB) is discharged by 50 mV from its initial high level [13]. The 50-mV differential between BL and BLB is good enough to be detected by a sense amplifier, thereby avoiding misread [13], [14]. It is observed that 6T and WRE8T have smallest read access time.

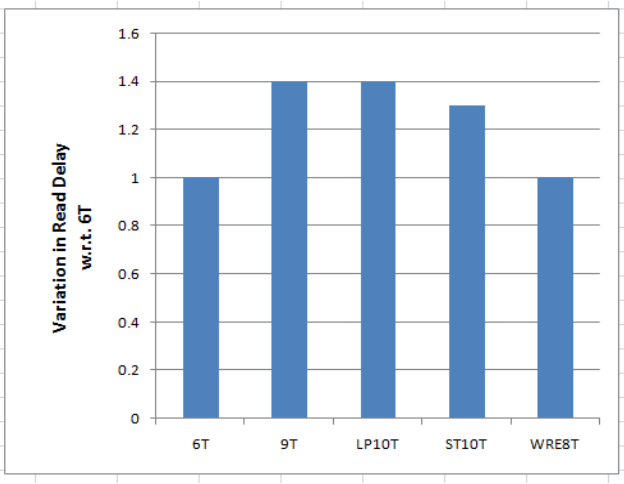

Fig 7: Comparison of read access time

3.3 Write Access Time(WAT)

Fig. 8 shows comparision of write access time. *T*WA (write access time or write delay) is estimated as the time required for writing “0” to storage node “L” from the time when WWL(WL) is activated to the time when “L” falls to 10% of its initial high level (i.e., its 90% swing). Similarly, *T*WA for writing “1” to “L” is estimated from the time when WWL (WL) is activated to the time when “L” rises to 90% of its full swing from its initial low level. This avoids miswrite. All the SRAM cell shows small and equal write access time except WRE8T.

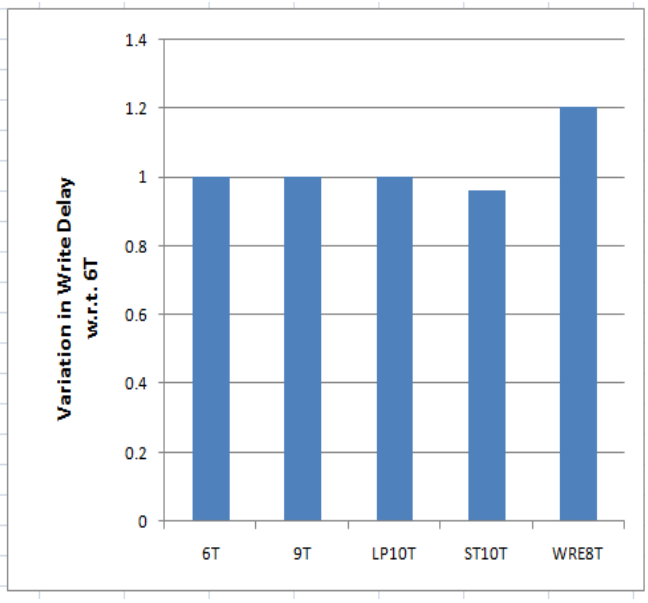

Fig 8: comparison of write access time

3.4 Layout Area

Fig. 9 shows comparison of layout area. It is observed that 6T has smallest layout area. Layout area provide information about bit line capacitance, internal node capacitance, read access time, write access time and packaging density of SRAM.

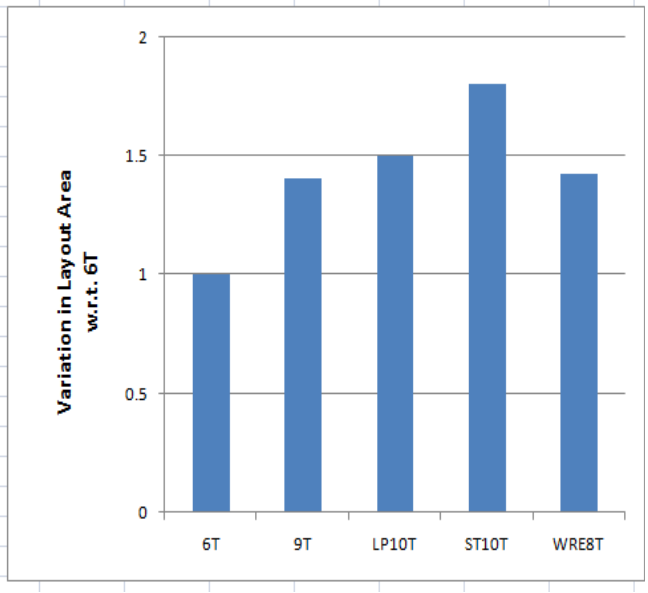

Fig 9: comparison of layout area

3.5 Result Analysis

Complete characterization on microwind performed at 90nm MOS technology. SRAM cells are compared on the basis of following parameter like Read Access Time(RAT), Write Access Time(WAT), Write Power and Layout Area as shown in table-1.

Table-1: result analysis on microwind

SRAM Parameters	6T	9T	LP10T	WRE8T
Write Power(uW)	1.848	1.967	1.773	0.755
Read Access Time(psec)	23.64	28.99	28.99	29.38
Write Access Time(psec)	257	181	164	514
Layout Area(um^2)	3.42	5.13	5.13	5.31

4. CONCLUSION

The most conventional way to reduce the power dissipation is the reduction of the supply voltage, reduce the size of MOS and insert tail transistor in SRAM cell. The power dissipation reduction in SRAM depends on supply voltage. Recently, silicon technology scaling demands a decrease in both Vdd and Vth to sustain delay reduction. As review earlier, research starts form 6T upto WRE8T. It is oberserved that low power and high speed SRAM cell required for SRAM array. Recently Proposed WRE8T SRAM cell occupy similar area like LP10T and 9T while occupies 50% more area than 6T. Similarly, WRE8T slower read operation with small write power as compare to 6T, 9T,LP10T and ST10T. Read access time of WRE8T is similar like 6T, 9T, LP10T and ST10T. One of the drawback of WRE8T is that slower write access time so that speed of SRAM operation reduces. The performance of SRAM can be improved further dynamic supply voltage scaling, which improves speed and power consumption.

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