

# A Comparative Study of Interconnection Network

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## ABSTRACT

The topology of interconnection networks the stage a key role in the performance of all general purpose networking applications. Cube-based architectures are one of the most important interconnection networks that focuses upon the evaluation and applications of cube-based networks. Cube-based architectures have received greatly focus over the past decade since they propose a wealthy interconnected structure with a number of attractive properties such as low diameter, high bisection width, smaller complexity and Cost. However, the major drawback of cube-based architectures is the difficulty of its VLSI layout. In Parallel computer, the hypercube network has been broadly used as the interconnection network. However, the number of communication links for each node is a logarithmic function of the total number of nodes in hypercubes. Therefore, the hypercube is not a superior applicant for an interconnection network for a extremely large parallel computer that might contain hundreds of thousands of nodes due to IC technology and port number restrictions. In this paper a variety of interconnection network based on the cube-based networks is brief discussed along with their properties. X-torus topology has better properties in terms of diameter, average latency, throughput, and path diversity. Although some more links are added in xtorus, the number of links is of the same order of magnitude with that of mesh, xmesh, and torus. It also takes advantage of increasing higher levels of VLSI process. The comparative study suggests the methods to overcome the above restrictions besides having attractive properties.

## General Terms

Parallel processing, Interconnection networks, Topological Properties

## Keywords

Performance evaluation, Diameter, Average node distance, Message Traffic density

## 1. INTRODUCTION

Parallel computing has become an essential subject in the field of computer science and has established to be critical when researching high performance computer. Parallel processing is information processing that emphasizes the concurrent manipulation of data elements belonging to one or more process solving a single problem. A parallel computer is a multiple processor computer capable of parallel processing. The throughput of a device is the number of results it produces per unit time [1][2][3]. There are many ways to improve the throughput of a device. The speed at which the device operates can be increased, or the concurrency the number of operations that are being performed at any one time can be increased. Parallel computing is largely based upon interconnection network topology. Interconnection network has been generally accepted to be the most realistic model of parallel computing [3][4][5]. On the other hand, when more

than one processor needs to access a memory structure, interconnection networks are needed to route data — 1. from processors to memories (concurrent access to a shared memory architecture), or 2. from one processing element (combination of processor and memory) to another (to present a message-passing architecture) [6][7][8]. The topology network can be either static or dynamic. Static network consist of point-to-point communication links among processing nodes that will not change once created. It is also referred as direct network such as linear, ring, mesh, cube architecture etc. dynamic network are built using switches and communication links are connected via switches to establish path among processing nodes and memory modules[9][10]. These networks are also referred as indirect network such as switching, routing technique etc. Interconnection networks (INCNs) play a central role in determining the overall performance of a multiprocessor system. To address the crisis of the performance of such networks extensive research has been made on different types of multiprocessors systems. Deciding the suitable network is an important problem in the design of parallel and distributed computers. In general, finding the optimal network to implement any parallel application does not have a known theoretical solution. There are many different ways to find efficient topologies that trade-off high level performance issues against various implementation constraints [11][12]. A topology is evaluated in terms of a number of performance parameters such as node, degree, diameter, bisection width, cost, average distance node and message traffic density. So, there are numerous researchers have developed different architectures which are considered better in terms of particular parameters.

In this paper, we describe the following section presents the topological properties of Interconnection networks and its variant networks. Sections 2 describe the different parameter networks used to make the topological evaluation. Various parameters used to compare the topological properties of interconnection networks and its variant networks are discussed in section 3, in section 4, describe the comparative study of the various architectures and finally concluded the paper in section 5.

## 1.1 Parameters of Interconnection Network

The several metrics are generally used to describe the performance of interconnection networks [3] [6]:

- **Degree or Connectivity ( $d$ )**, the number of edges (links) connected with a node (i.e., the number of nodes that can be reached from it in one hop).
- **Network Diameter ( $D$ )**, the diameter of network is the shortest path between any two nodes. The distance is measured in terms of number of distinct hops between any two nodes, diameter should be kept small.

- **Cost**, the cost of the network is in terms of the number of communication links required by the network (i.e. Cost= $d \cdot D$ ). This is broadly used in performance evaluation.
- **Average Node Distance**, where the distance between two nodes is defined by the number of hops in the smallest path between those nodes. Average distance is given by

$$d_{avg} = \frac{\sum_{d=1}^r (d \cdot N_d)}{N - 1}$$

where  $N$  is the number of nodes,  $N_d$  is the number of nodes at distance  $d$  apart, and  $r$  is the diameter.

- **Message Traffic Density ( $\rho$ )**, this factor is defined as  $\rho = d_{avg} N / E$ . Where  $E$  is the total number of links and  $d_{avg}$  is the average node distance.

## 2. INTERCONNECTION NETWORKS

### 2.1 Hypercube (HC)

The hypercube has been broadly used as the interconnection network in a wide variety of parallel systems such as Intel iPSC [24], the nCUBE [21], the Connection Machine CM-2 [22] and SGI Origin 2000 [23]. An  $n$ -dimensional hypercube or  $n$ -cubes equal to  $2^n$  nodes and has  $n$  links per node. If single  $n$ -bit binary addresses are assigned to the nodes of an  $n$ -dimensional hypercube, then a link connects two nodes if and only if their binary addresses change in a single bit. Because of its elegant topological properties and the ability to emulate a broad variety of other frequently used networks, the hypercube has been one of the most popular interconnection networks for parallel computer systems. However, the number of edges per node increases logarithmically as the total number of nodes in the hypercube increases. The hypercube has a high bisection width  $2^{n-1}$  and has high-quality potential of fault tolerance [4] [5] [6].

### 2.2 Metacube (MC)

The MC network is provoked by the dual-cube network [20] that mitigates the port restriction problem in the hypercube network so that the number of nodes in the network is much superior to that of the hypercube with a fixed number of links per node. The MC network includes the dualcube (DC) as a special case. The MC network has a 2-level cube structure: a high-level cube represented by the leftmost  $k$  bits of the binary address of the node which contains  $m2^k + k$  bits and low-level cubes, called clusters that forms the basic component in the network, represented by the  $m$  bits of the remain  $m2^k$  bits, which occupy the different portion of the  $m2^k$  bits for the different classes [4]. The MC is a symmetric network shown in fig. 1.

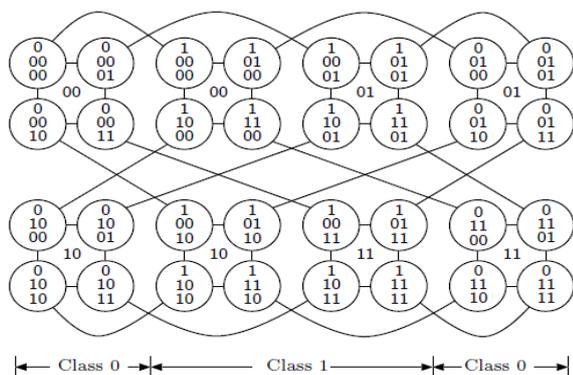


Fig.1 A Metacube MC (1, 2)

### 2.3 Crossed Cube (CC)

$CC_n$  represented as an  $n$ - dimensional crossed cube, is obtained by passage some edges in an  $n$ -dimensional Hypercube. The Crossed Cube has the same vertex and edge complexity as the Hypercube but only about half of diameter, wide diameter, and fault-diameter as the Hypercube with the same dimension [9]. Average distance between vertices is smaller and it can simulate a Hypercube through dilation 2 embedding. The construction is  $CC_n$  from a hypercube by changing the way of connection of few hypercube links [10]. And the diameter of  $CC_n$  is half of the diameter of the hypercube, or more quite, it is  $d \lceil (n+1)/2 \rceil$  for a network containing  $2^n$  nodes. The  $CC_n$  is an  $n$ -regular graph of  $2^n$  nodes [11]. In Each node,  $CC_n$  is recognized by an exclusive binary string of length  $n$ . The connectivity of node is  $n$  in crossed cube, the bisection width is  $2^{n-1}$  and the number of edges is  $n \cdot 2^{n-1}$ .  $CC_n$  shown in Fig. 2 is similar to hypercube.

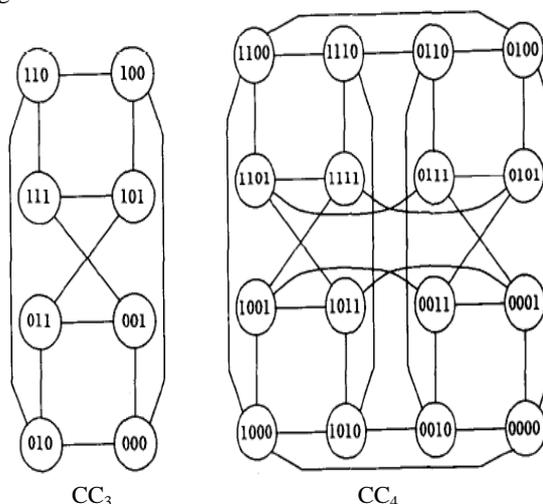


Fig. 2  $CC_n$  for  $n=3$  and 4

### 2.4 Folded Crossed Cube (FCC)

The Folded crossed cube is constructed by linking every node to a node utmost from it. Figure 3(a) and (b) respectively describe the structure of FCC of dimension 3 and 4. In fig 3(b) all the opposite links of FCC4 are not shown for straightforwardness. The FCC is a graph  $F_r(V, E)$  with the identical set of vertices as in CC and with the edge set  $E$  that is a super set of  $E$ . There are two different views of folded cross cubes as shown in Fig. 3. The  $FCC_3$  indicates three dimensions FCC and  $FCC_4$  indicate a four dimension FCC. In dimension four Folded Crossed Cube, all the opposite links of FCC (4) are not shown for simplicity [12].

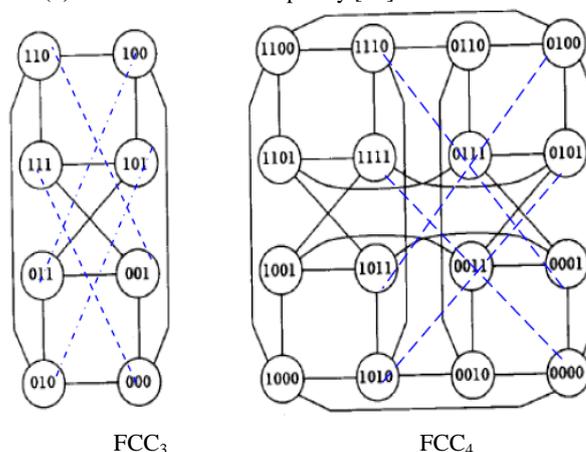


Fig. 3  $FCC_n$  for  $n=3$  and 4

### 2.5 Star Vertical Cube (SVC)

A network Star vertical cube in which Varietal hypercubes are connected in Star graph fashion. An  $m$  dimensional Varietal hypercube can be modeled as a graph with the node set  $V_m$  and edge set  $E_m$ , where  $|V_m| = 2^m$  and  $|E_m| = m \times 2^m$ . The  $2^m$  nodes are definitely addressed by  $m$ -bit binary numbers, by values from 0 to  $2^m - 1$ . Each node has link at  $m$ -dimensions, ranging from 1 (lowest dimension) to  $m$  (highest dimension), connecting each node to  $m$  neighboring nodes [14].

Both the Varietal hypercube VC ( $m$ ) and the Star ( $n$ ) are regular, vertex (edge) symmetric. SVC ( $n, m$ ) of order ( $n, m$ ) is the multiple graph of S ( $n$ ) and VC ( $m$ ). Given a node  $\langle x, y \rangle$  of the SVC ( $n, m$ ),  $x$  will be called the varietal hypercube part label and  $y$  the star-graph part label. It is remarkable that the nodes with the identical varietal hypercube part label form an  $n$ -star whereas the nodes with the same star-graph-part label form a varietal hypercube of order  $m$  [19]. It follows that there are  $n!$  Varietal hypercube sub graphs VC ( $m$ ) in the SVC ( $n, m$ ) where, the nodes in each VC ( $m$ ) have the same star-graph-part label. These sub graphs can be recognized by their corresponding star-part-label as shown in Fig.4.

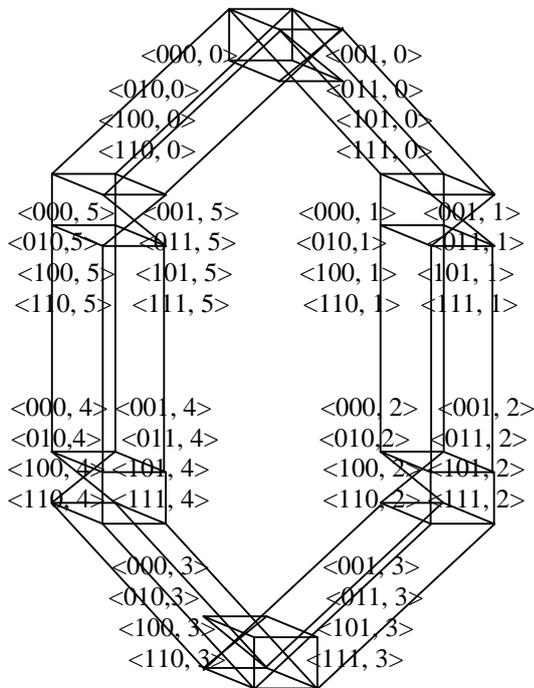


Fig. 4 A Star Vertical Cube SVC (3)

### 2.6 X-Torus

X-torus network is a two-dimension topology. This network can be located in an X-Y frame and every node is indicates as  $(a,b)$ . A  $k_x \times k_y$  X-torus network is a graph  $G=(N, C)$ , defined as:  $N = \{(a,b) \mid 0 \leq a \leq k_x, 0 \leq b \leq k_y\}$

where  $k_x \geq 2, k_y \geq 2, (u_a, u_b)$  and  $(v_a, v_b)$  are the coordinates of the nodes  $u$  and  $v$  respectively.

In Fig.5, the X-torus architecture use links to attach the node  $(a,b)$  and the node  $([a + \lfloor k/2 \rfloor]_k, [b + \lfloor k/2 \rfloor]_k)$ . The degree of X-torus is dependent on the parity of  $k$ . The degree is 5, when  $k$  is even, the degree is 6, when  $k$  is odd. When  $k$  is even, the link that connects the node  $(a, b)$  and the node  $([a + \lfloor k/2 \rfloor]_k, [b + \lfloor k/2 \rfloor]_k)$  is the same with the link that connects the node  $([a + \lfloor k/2 \rfloor]_k, [b + \lfloor k/2 \rfloor]_k)$  and the

node  $([a + \lfloor k/2 \rfloor]_k + \lfloor k/2 \rfloor, [b + \lfloor k/2 \rfloor]_k + \lfloor k/2 \rfloor)$ . Therefore, the degree for even  $k$  is lesser than that for odd  $k$  [15, 16].

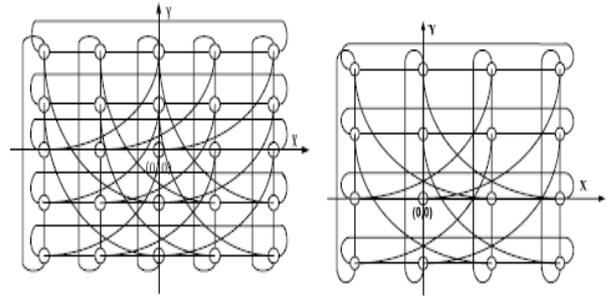
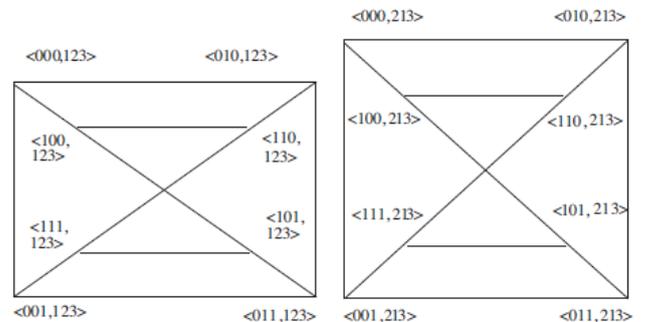


Fig. (a) 5x5 X-Torus (b) 4x4 X-Torus

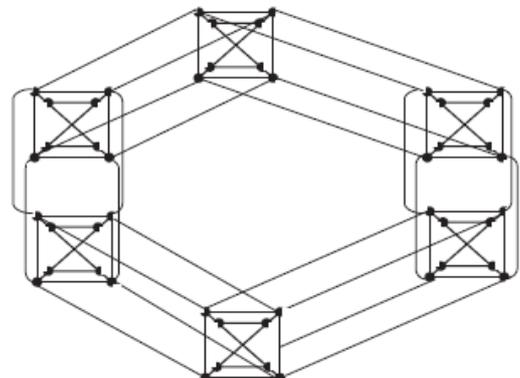
### 2.7 Star Crossed Cube (SCC)

The SCC ( $k,m$ ) is the multiple graph of the CC( $m$ ) and  $n$ -dimensional star graph S( $n$ ). That is, in an  $n$ -star, every vertex is shift with a CC. Next, the node address of every vertex in the resultant graph will have 2 parts  $\langle P_{m-1}; P_{m-2} \dots P_0, Q_0; Q_1, \dots, Q_{n-1} \rangle$ , where the  $P_i$  s represent the CC part and the  $Q_i$  s represent the star part. Each node will have 2 types of neighbors, namely the CC-part neighbor and star-part neighbor with node addresses  $\langle P_{m-1}; P_{m-2} \dots P_i', Q_0; Q_1, \dots, Q_{n-1} \rangle$  and  $\langle P_{m-1}; P_{m-2} \dots P_0, Q_i, Q_{i-1}, Q_0, \dots, Q_{n-1} \rangle$ , respectively. The SCC (3,3), along with the submodules, is shown in Fig. 6a, 6b, and 6c, respectively. In Fig. 6a, the first submodule with the star part labeled as 123 and the corresponding labels of the CC are shown. Similarly, Figure 6b shows the second submodule of the SCC (3,3) with 213 as their star part level [18]. The total number of nodes and degree in the SMC ( $k,m$ ) graph are  $k!2^m$  and  $m+k-1$  respectively.



SCC123 (a)

SCC213 (b)



SCC (3,3) (c)

Fig.6 The SCC and its basic modules: (a) SCC123 (b) SCC213 (c) SCC (3, 3)

### 2.8 Star Mobius Cube (SMC)

The Star mobius cube represented as SMC (k,m) is the product graph of m-Star S(m) and K-mobius cube MQ<sub>k</sub>. Here, each node of star graph is substituted by mobius cube. The address of every node in SMC has two parts Xi that represents star part and Yi represents MQ part {x<sub>0</sub>x<sub>1</sub>...x<sub>n</sub>y<sub>k-1</sub>y<sub>k-2</sub>...y<sub>0</sub>}.

In simple logic, mobius cubes are placed on star platform. The Fig. 7 illustrates the Star-Mobius cube topology SMC (3,3) for dimension 3. The total number of nodes and degree in the SMC (k,m) graph are k!2<sup>m</sup> and m+k-1 respectively. The total number of edges in the SMC (k, m) is also k! 2<sup>m-1</sup> (k + m - 1) [17].

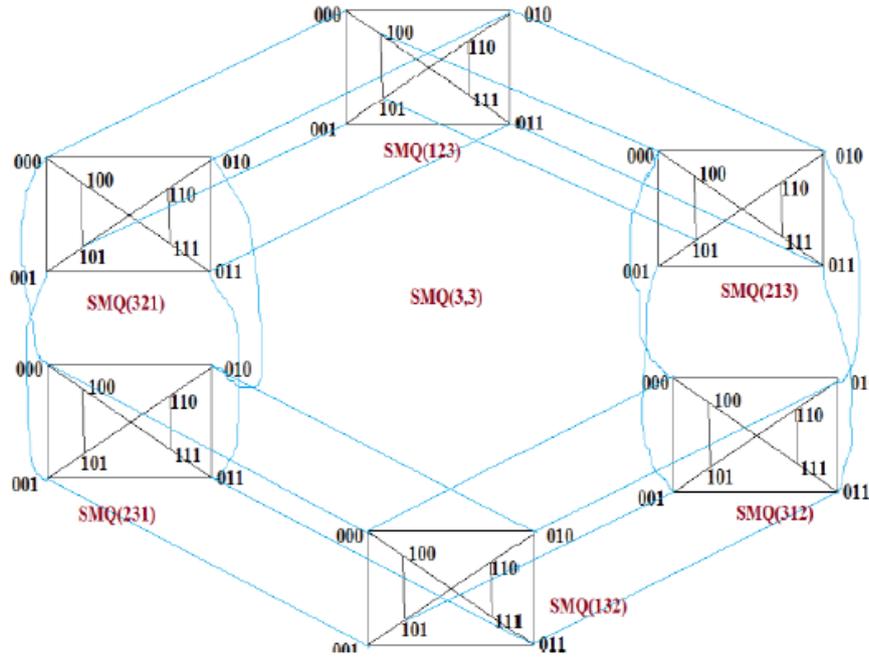


Fig. 7 The Star Mobius Cube

### 3. PARAMETERS OF INTERCONNECTION NETWORK

The Various parameters of Interconnection networks along with the network properties are summarized in Table 1.

Table 1. Comparison of parameters of various architectures

Networks	Nodes	Degree (d)	Diameter (D)	Cost	Average Distance Node	Message Traffic Density
HC	2 <sup>n</sup>	n	n	n <sup>2</sup>	$\frac{n}{2}$	$\frac{dN}{E} \approx 1$
MC (k,m)	2 <sup>n</sup>	m + k	2 <sup>k+1</sup>	$(m + k) \times (m + 1)2^k$	$d_{avg} \leq 2^k \left( \frac{m}{2} + 1 \right)$	$\frac{d_{avg} N}{E}$
CC	2 <sup>n</sup>	n	$\left\lceil \frac{(n+1)}{2} \right\rceil$	$n \times \left\lceil \frac{(n+1)}{2} \right\rceil$	$\bar{d}_{2k}$	$\frac{\bar{d}_{2k} N}{E}$
FCC	2 <sup>2n</sup>	n + 1	$\left\lceil \frac{n}{2} \right\rceil$	$(n + 1) \times \left\lceil \frac{n}{2} \right\rceil$	$\bar{d}$	$\rho = \frac{\bar{d} N}{E}$
SVC (n,m)	n! 2 <sup>m</sup>	m+n-1	$\left\lceil \frac{2m}{3} \right\rceil + \left\lceil \frac{3}{2}(n-1) \right\rceil$	$(m + n - 1) \times \left( \left\lceil \frac{2m}{3} \right\rceil + \left\lceil \frac{3}{2}(n-1) \right\rceil \right)$	$\bar{d}_k$	$\rho = \frac{\bar{d}_k N t}{E}$
X Torus	Even k <sup>2</sup>	5	$\left\lceil \frac{k}{2} \right\rceil$	$5 \left\lceil \frac{k}{2} \right\rceil$	$D_{XE}$	$\frac{D_{XE} N}{E}$
	Odd k <sup>2</sup>	6	$\left\lceil \frac{k}{2} \right\rceil + 1$	$6 \left( \left\lceil \frac{k}{2} \right\rceil + 1 \right)$	$D_{XO}$	$\frac{D_{XO} N}{E}$

SCC (k,m)	$k! 2^m$	$m+k-1$	$\left\lceil m + \frac{1}{2} \right\rceil + \left\lfloor \frac{3}{2}(k-1) \right\rfloor$	$(m+k-1) \times \left( \left\lceil m + \frac{1}{2} \right\rceil + \left\lfloor \frac{3}{2}(k-1) \right\rfloor \right)$	$\bar{d}_{av} = \left( \frac{11x+4y}{8} \right) + \left( k - 4 + \frac{2}{k} + \sum_{i=1}^k \frac{1}{i} \right)$	$\frac{2\bar{d}_{av}}{m+k-1}$
SMC (k,m)	$k! 2^m$	$m+k-1$	$\left\lceil \frac{m+1}{2} \right\rceil + \left\lfloor \frac{3}{2}(k-1) \right\rfloor$	$(m+k-1) \times \left( \left\lceil \frac{m+1}{2} \right\rceil + \left\lfloor \frac{3}{2}(k-1) \right\rfloor \right)$	$d \leq m/3 + [1 - (-1/2)^m]/9 + 1 + k - 4 + (2/k) + \sum_{i=1}^k \frac{1}{i}$	$\frac{2\bar{d}_{av}}{m+k-1}$

#### 4. COMPARATIVE STUDY OF VARIOUS ARCHITECTURE

This section evaluates different parameters of various architectures and a comparison is made with other networks. Different interconnection parameters are compared in Table 1. The nodes, degree, diameter and cost, average node distance, message traffic density of various architectures have been compared with that of HC, MC, CC, FCC, SVC, X-TORUS, SCC and SMC. We continue to take into account the four essential parameters such as number of processors, diameter, average node distance and message traffic density. The curves are plotted for every of the parameters of interconnection networks. Fig. 8 shows the increasing number of processors for each level of the extensible. Now, we can see that the hypercube and crossed cube, SVC, SCC and SMC are same but X-Torus has smaller number of processors. Therefore, the difficulty of X-torus network is smaller, when they are increasing on higher level. However, the cube based architectures have exponential expansions which make the network highly complex.

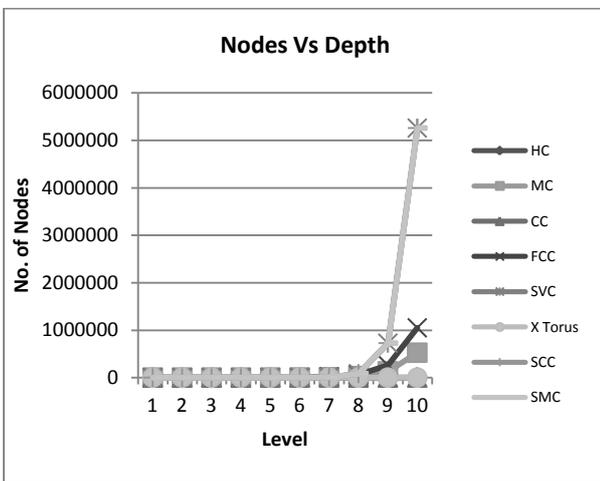


Fig.8 Comparison of various architectures

When testing the performance of various interconnection networks in terms of diameter, the Folded Crossed Cube (FCC) has lesser diameter as compare to other types of architectures as shown fig. 9.

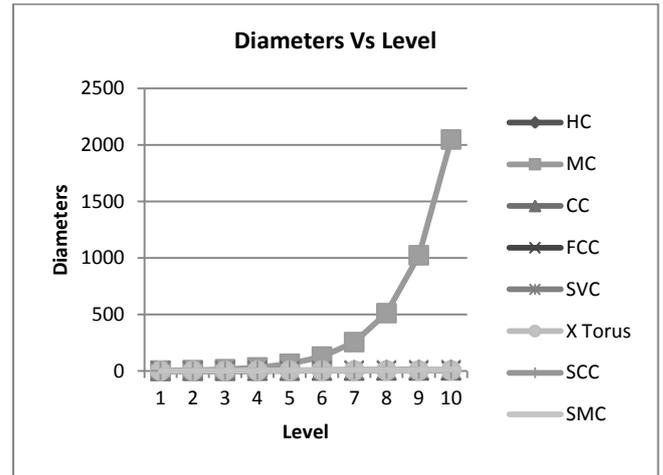


Fig.9 Comparison of various architectures

When evaluating the performance of various interconnection networks in terms of average distance node, the X-Torus is to be found quite reduced as shown in fig. 10.

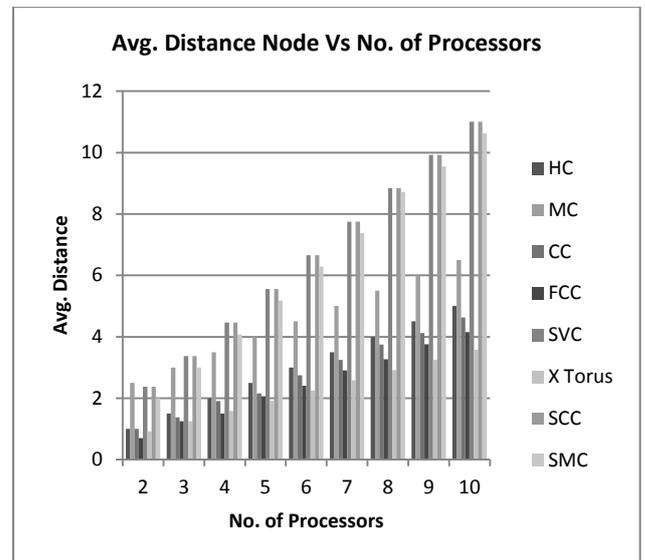


Fig.10 Comparison of Avg. Distance Node on various architectures

The message traffic density is also evaluated for HC, MC, CC, FCC, SVC, X-Torus, SCC and SMC. The comparison as shown in fig.11. It is observed that the Metacube (MC) is always decreasing the value of message traffic density, when we are increasing the number of processors.

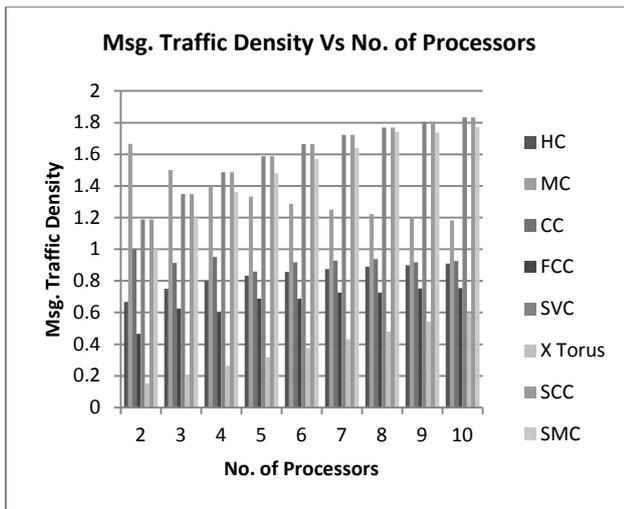


Fig. 11 Comparison of Message Traffic Density on various architectures

## 5. CONCLUSION AND FUTURE SCOPE

This paper reviews the performance of various multiprocessor architectures by taking into account their topological properties. The comparative study of various types of interconnection network is made in term of parameter. In interconnection networks, it is evaluated that the X-Torus is giving better performance in terms of nodes and average nodes distance. FCC and MC have shown better performance in terms of diameter and message traffic density respectively. The option of the interconnection network may affect numerous characteristics of the system such as node complexity, bisection width, scalability and cost of network etc. The current study is carried out on the basis of numerous characteristics a variety of multiprocessor interconnection networks. There have been more work related to design of suitable multiprocessor network. Yet, no one claim a particular design which well-established all the attractive properties. The current study gives many scopes to design high performance interconnection network that can be used in designing of multiprocessor server.

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## 7. REFERENCES

- [1] C. 'obal A. Navarro, N. Hitschfeld-Kahler and Luis Mateu "A Survey on Parallel Computing and its Applications in Data-Parallel Problems Using GPU Architectures" Vol. 15, No. 2, pp. 285-329, 2014.
- [2] S. Patel, P. Parandkar, S. Katiyal and A. Agarwal, "Exploring Alternative Topologies for Network-on-Chip Architectures," BIJIT - BVICAM's International Journal of Information Technology Vol. 3, No. 2, ISSN 0973 – 5658, 2011
- [3] N. Adhikari, C. R. Tripathy "The Folded Crossed Cube: A New Interconnection Network for Parallel Systems", International Journal of Computer Applications (0975 – 8887) Vol. 4, No.3, 2010
- [4] Y. Li, S. Peng and W. Chu "Metacube – A New Interconnection Network for Large Scale Parallel Systems" ACSAC02, Australian Computer Science Communications, Vol.24, No.4, pp. 29–36, 2001.
- [5] Y. Saad and M. H. Schultz "Topological properties of Hypercube" IEEE Trans. Computer. Vol.37, No. 7, pp. 867–872, 1988.
- [6] Z. A. Khan, J. Siddiqui and A. Samad "Topological Evaluation Of Variants Hypercube Network" Asian Journal of Computer Science And Information Technology Vol. 3, No.9, pp. 125 – 128, 2013.
- [7] A., A.E and S. Latifi, "Properties and performance of folded hypercubes," IEEE Transactions on Parallel and Distributed Systems, Vol. 2, pp. 31-42, 1991.
- [8] N. Adhikari, C. R. Tripathy "On A New Interconnection Network for Large Scale Parallel Systems" International Journal of Computer Applications (0975 – 8887) Vol. 23, No.1, 2011.
- [9] C. P. Chang, T. Y Sung, and L.H. Hsu, "Edge congestion and topological properties of Crossed cube," IEEE Trans. Parallel and Distributed Systems, Vol. 11, No. 1, pp. 64–80, 2000.
- [10] K. Efe, P. K. Blackwell, W. Slough, and T. Shiau, "Topological Properties of the Crossed Cube Architecture," Parallel Computing, Vol. 20, pp. 1,763–1,775, 1994.
- [11] P. Kulasinghe and S. Bettayeb, "Embedding binary trees into Crossed cube," IEEE Trans. Computers, Vol. 44, No. 7, pp. 923–929, 1995.
- [12] N. Adhikari, C. R. Tripathy "The Folded Crossed Cube: A New Interconnection Network for Parallel Systems", International Journal of Computer Applications (0975 – 8887) Vol. 4, No.3, 2010.
- [13] J. Alam, R. Kumar and Z. Khan "Linearly Extendible Arm (Lea) – A Constant Degree Topology for Designing Scalable and Cost Effective Interconnection Networks" Ubiquitous Computing and Communication Journal.
- [14] B. Nag, D. Pradhan, N. K. Swain and N. Adhikari, "Star varietal cube: A New Large Scale Parallel Interconnection Network", International Journal Communication & Network Security (IJCNS), Vol. 1, Issue-II, 2011.
- [15] H. Gu, Q. Xie, K. Wang and J. Zhang, and Y. Li "X-Torus: A Variation of Torus Topology with Lower Diameter and Larger Bisection Width".
- [16] L. Y. Hang, Z. Ming-fa, W. Jue, X. Li-min and G. Tao, "Xtorus: An Extended Torus Topology for On-Chip Massive Data Communication," 26th IEEE Int. Parallel and Distributed Processing Symposium Workshops & PhD Forum (IPDPSW), pp. 2061-2068, 2012.
- [17] D. Pattanayak, D. Tripathy and C.R.Tripathy "Star-Mobius Cube: A New interconnection Topology for Large Scale Parallel Processing" International Journal of

Emerging Technologies in Computational and Applied Science (IJETCAS).

- [18] N. Adhikari and C. R. Tripathy “Star-crossed cube: an alternative to star graph” *Turkish Journal of Electrical Engineering & Computer Sciences* 22: pp.719-734, 2014.
- [19] S. B.Akers, D. Harel and B. Krishnamurty, “The Star Graph: An AttractiveALternative to the n-Cube” in *Proc. Int. Conf. Parallel Processing*, pp. 393-400, 1987.
- [20] Y. Li and S. Peng, “Dualcube: A New Interconnection Network for High-Performance computer Clusters,” *International computer symposium, workshop on Computer architecture*. pp. 6-8, 2000.
- [21] H., J.P., and Mudge, T.N., “HyperCube Supercomputer”, *the IEEE*, Vol. 72(12), pp.1829-1841, 1989.
- [22] L. W. Tucker and G.G. Robertson, “Architecture and Applications of the Connection machine”. *IEEE computer*, pp. 26-38, 1988.
- [23] Aad J. van der Steen and Ruud van der Pas “A performance analysis of SGI Origin 2000”, in *proceeding of Vecpar 98*, pp. 319-332, 1998.
- [24] J. Wiley. Vanvoorst, B., Seidel, S., and Barszcz, E. “Workload of an iPSC/860”. In *Proc. Scalable High-Performance Computing Conf*, pp. 221-228, 1994.