Performance Analysis of FinFET based Carry save Adder Cell with Predictive Technology Models

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ABSTRACT
As scaling of conventional metal-oxide-semiconductor field effect transistor is approaching its fundamental and technological limits, alternate device solutions are being developed. FinFET is rapidly replacing conventional CMOS transistors as it offer lot of improvements in power consumption, propagation delay and propagation delay product (PDP). This paper presents design & simulation of a double gate FinFET based ultra low power 2-bit Carry Save Adder (CSA) cell. A comprehensive comparison of FinFET and CMOS based 2-bit carry save adder has been performed. The CMOS & FinFET based 2-bit carry save adder circuits are evaluated at 32nm & 45nm nanoscale technology nodes using Predictive Technology Models (PTM). At 45nm technology node, the FinFET based carry save adder results shows average power consumption reduction of 39.75%; propagation delay reduction of 92.50% and a propagation delay product (PDP) improvement of 94.42% as compared to CMOS counterparts. The FinFET based carry save adder results shows average power consumption reduction of 42.19%; propagation delay reduction of 86.86% and a propagation delay product (PDP) improvement of 92.22% as compared to CMOS based carry save adder at 32nm technology node.

Keywords
CMOS, FinFET, CSA, PDP, AND, XOR, OR, Double-gate.

1. INTRODUCTION

Microprocessor is the important element in the digital circuit design. The arithmetic unit of microprocessor consist of adders as one of the basic element. Among various adders, carry save adder (CSA) has lowest PDP. Nowadays, the major concerns required in the designing of the digital circuits are in the field of power dissipation and propagation delay. PDP is one of the most important performance metric in digital circuit design. As the CMOS devices are scaling day by day, this leads to short channel effects, process reliability degradation and process variation. In order to overcome these problems, new technologies are adopted like FinFET. The FinFET have multi-gate structure which improves mobility, negligible short channel effects, minimum random dopant fluctuations, reduced parasitic junction capacitance and hence improved area efficiency [1-7].

Double Gate FinFET has two gates, one is front gate and other is back gate, it provides flexibility in design with low power and delay. Due to its low leakage structure, the current strength ratio also improves [8-12]. FinFET top and cross-sectional view is demonstrated in fig. 1(a) and (b) respectively.

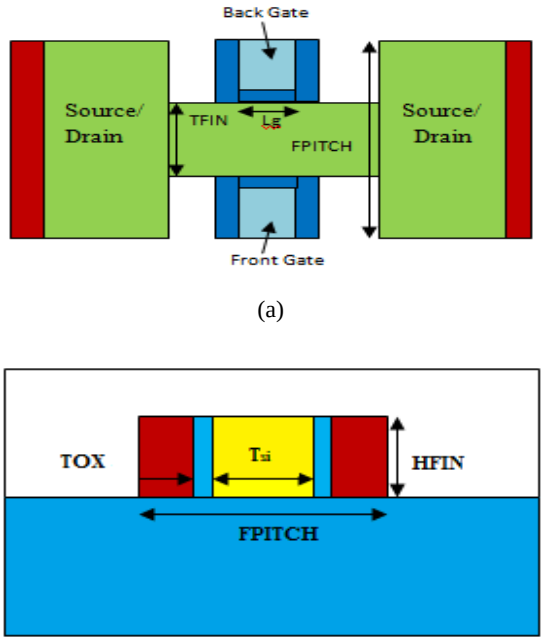

Fig. 1(a) Top View of FinFET (b) Cross-sectional view of FinFET

Figure 1(b) shows a FinFET multi-fin structure, where T_{si} represents the thickness of thin silicon body of the fin which is connected to gate electrodes. The channel is upright to the hydroplane of the wafer and current is parallel to hydroplane of the wafer. The front gate and back gate becomes control independent by etching away electrode gate from the top of the channel. The effective gate width of FinFET is given as ***2*n*h***; where, h is the height and n is number of fins in the structure.

Doped channel FinFETs are suitable for system on chip (SOC) which need multiple threshold voltages on the same die because back gate of FinFET can be used to adjust threshold voltages. For a non planner device structure, FinFET technology is better replacement in terms of efficiency [13-17].

For predictive modeling, Berkeley Predictive Technology Model (BPTM) was developed for multi-gate transistor

FinFET using the Berkeley common multi-gate (BSIMMG). HP (high performance) PTM models for 32nm & 45nm technology nodes have been used for CMOS & MGTMOS (Multi Gate Transistor MOS) [18-20].

2. CARRY SAVE ADDER DESIGN

A 2-bit CSA circuit is designed that have low power consumption and delay. The simulation of 2-bit CSA circuit is carried out using H-SPICE simulation tool. The CSA circuit consists of 4 XOR gates and 3 AND gates as shown in the fig. 2. The a_0, a_1, b_0 and b_1 are inputs of CSA and s_0, s_1 and s_2 are outputs where s_0 is least significant bit (LSB)) and s_2 is most significant bit (MSB) and VDD and GND are the power supply rails used in the circuit.

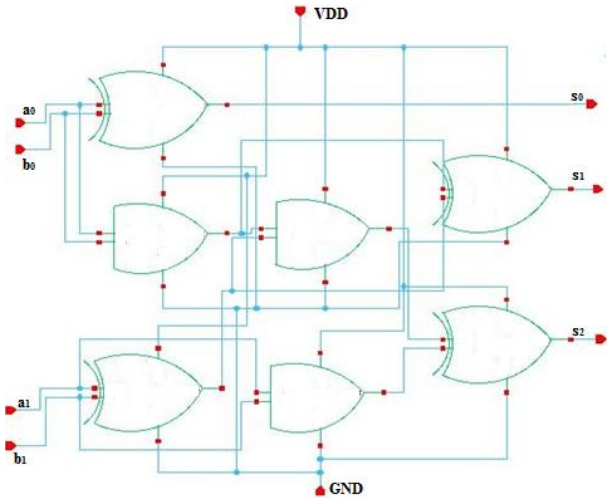

Fig. 2: Two Bit Carry Save Adder

Table 1 is the truth table of designed 2-bit CSA. Various possible input combinations are taken and the output waveform is shown in fig. 3.

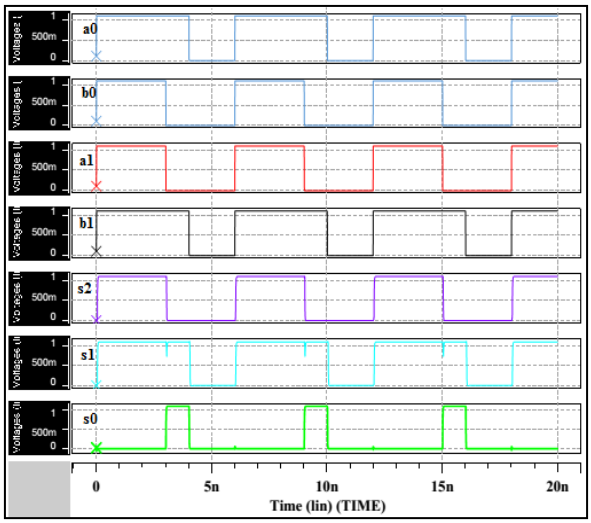

Fig. 3 Output waveform of 2-bit CSA

2.1 CMOS Based Carry Save Adder

CSA has basically two building blocks i.e. XOR and AND gates. The XOR gate is used to get SUM as output in adder circuit. XOR circuit consists of 8 NMOS and 8 PMOS transistors as shown in the fig. 4. Similarly AND gate is used to get carry as output. It consists of 3 PMOS and 3 NMOS transistors as shown in Fig. 5.

Table 1. 2-bit Carry save adder truth table

Inputs				Output		
a0	b0	a1	b1	s0	s1	s2
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	0	1
0	1	0	0	0	0	1
0	1	0	1	1	1	0
0	1	1	0	1	1	0
0	1	1	1	1	0	1
1	0	0	0	1	0	0
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	1	0	1
1	1	0	0	0	1	0
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	1

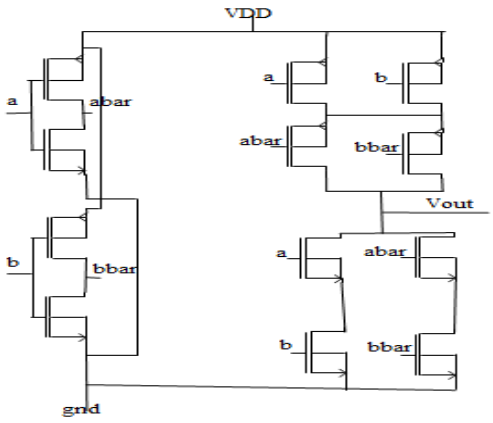

Fig. 4 CMOS based XOR gate

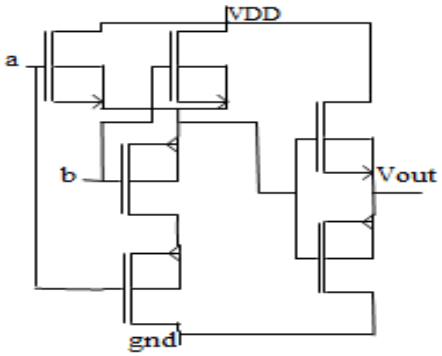

Fig. 5 CMOS based AND gate

2.2 FinFET Based Carry Save Adder

Double Gate (DG) FinFET transistors are used to design 2-bit CSA cell. The front and back gate of DG FinFET has self determining control which can be efficiently used to design high performance and low power circuits. For self-determining gate control, front and back transistors are connected. DG FinFET have back gate which makes it different from conventional CMOS transitors, hence reduces leakage current and short channel effects. There are two modes of operation in FinFET viz. Independent Gate (IG) and Short Gate (SG). In the IG FinFETmode, front gate and back gate is connected by different signal, it has five terminals-front gate, back gate, drain, source and bulk. In the SG FinFET front gate and back gate are connected together hence it has four terminals-gate, drain, source and bulk similar to conventional CMOS transistor. The FinFET based schematic design of 2-bit XOR gate and AND gates are shown in Fig. 6 and 7 respectively.

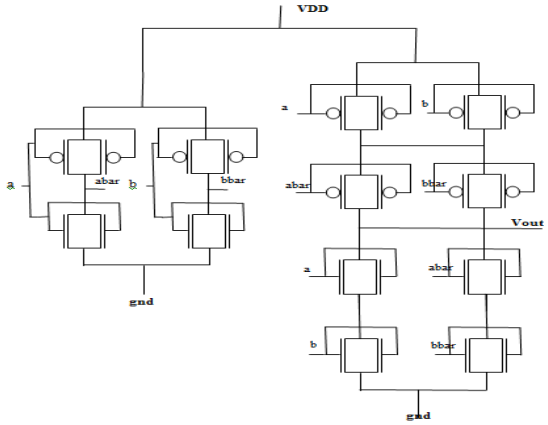

Fig. 6 Schematic design of FinFET based XOR gate

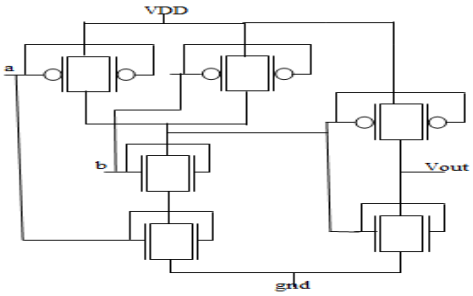

Fig. 7 Schematic design of FinFET based AND gate

3. RESULTS & DISCUSSIONS

3.1 Simulation results of basic N-type Transistor

The table 2 shows comparison of n-type transistor for CMOS and FinFET technologies at 45nm and 32nm nodes.

Table 2. Performance comparison of CMOS and FinFET based n-type transistor at 45nm and 32nm node

N-Type Transistor Parameter	45nm CMOS	45nm FinFET	32nm CMOS	32nm FinFET
Length(nm)	50	50	40	40
Width(nm)	200	200	160	160
V_{dd}(volt)	1.1	1.1	0.9	0.9
I_{ds}(µA)	275	525	170	310

Maximum drain current in n-type FinFET transistor is 525µA, while it is 275µA in conventional n-type CMOS at 45nm technology node i.e. n-type FinFET transistor provides 47% more drain current. At 32nm technology node, maximum drain current in n-type FinFET transistor is 310µA, while it is 170µA in conventional n-type CMOS i.e. n-type FinFET transistor provides 42% more drain current. Supply voltage (V_{dd}) is 1.1V for 45nm node and 0.9V for 32nm node. The bar graphs in fig. 8 shows the comparison of maximum drain current at 45nm and 32nm technologies for n-type FinFET and the CMOS transistors.

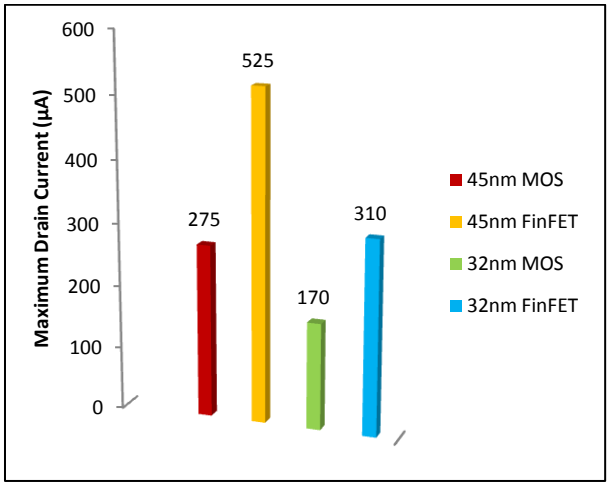

Fig. 8 Comparison of maximum drain current for CMOS & FinFET n-type transistors at 45nm and 32nm technologies

3.2 Carry Save Adder

The table 3 lists simulation results for CMOS & FinFET based carry save adder results at 45nm and 32nm technology nodes respectively. It is observed that there is 40.07%& 42.19% reduction in average power in FinFET based carry save adder as compared to conventional CMOS based carry save adder at 45nm & 32nm technology nodes respectively. Propagation delay reduction is 92.5% & 86.55% and power-delay product improvement is 94.40% & 91.79% in FinFET based carry save adder at 45nm & 32nm technology nodes. Fig. 9, 10 and 11 shows the bar-graph comparison of average power, propagation delay & power-delay product (PDP) at 45nm and 32nm nodes in the CMOS & FinFET technologies based CSA respectively.

Table 3. Performance comparison of CMOS and FinFET based 2-bit Carry Save Adders at 45nm and 32nm node

Parameter	**CMOS (45nm)**	**FinFET (45nm)**	**CMOS (32nm)**	**FinFET (32nm)**
Avg. Power(µW)	24.36	14.60	14.09	8.145
Propagation Delay(ns)	0.520	0.039	0.119	0.016
PDP(fJ)	12.67	0.582	1.670	0.137

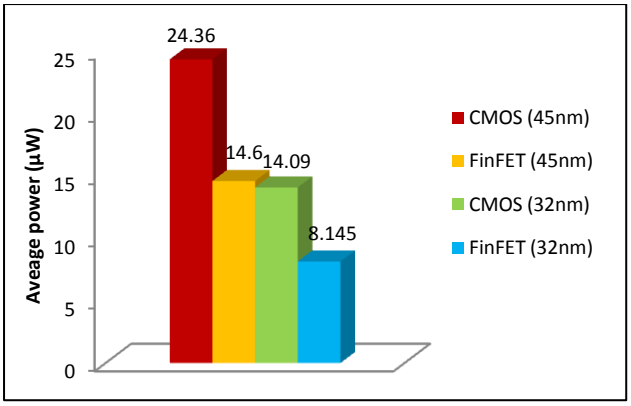

Fig. 9 Comparison of average power of FinFET and CMOS based CSA at 32nm & 45nm technology nodes

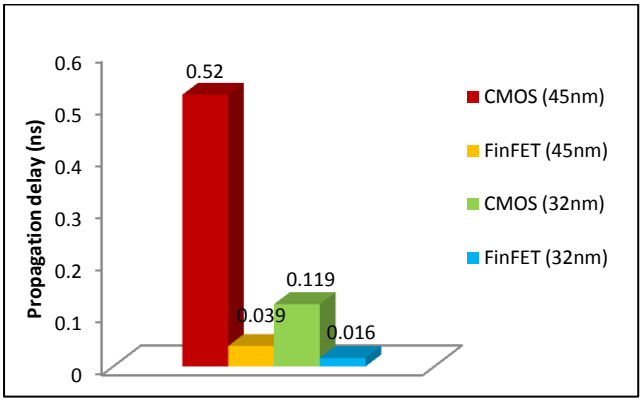

Fig. 10 Comparison of propagation delay of FinFET and CMOS based CSA at 32nm & 45nm technology nodes

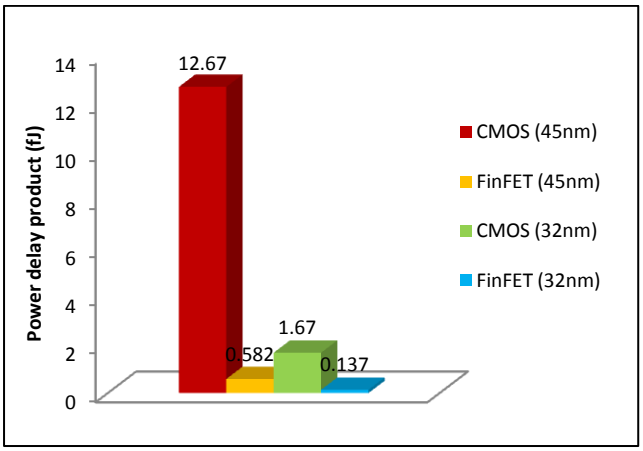

Fig. 11 Comparison of power-delay product of FinFET and CMOS based CSA at 32nm & 45nm technology nodes

4. CONCLUSION

As the FinFET offers lower leakage current and power dissipation; it became most favorable device beyond 22nm technology node. As an emerging new technology, FinFET offers many dimensions where research work can be explored. So, a carry save adder is designed using FinFET transistors and carried out its comparison with its CMOS counterpart. In this research work, the comparative analysis of circuits based on FinFET and CMOS technologies at 45nm and 32nm has been performed using H-SPICE tool. The predictive technology models (PTM) are used for simulation & analysis of CMOS and FinFET based 2-bit carry save adder circuits at 32nm & 45nm nanoscale technology nodes. FinFET based carry save adder results shows average power consumption reduction of 39.75% and 42.19%; propagation delay reduction of 92.50% and 86.86% and a propagation delay product (PDP) improvement of 94.42% and 92.22% as compared to CMOS counterparts at 45nm and 32nm technologies respectively. The results verified that FinFET technology outperforms CMOS technology in terms of power consumption, delay and power-delay product (PDP).

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