An Efficient VLSI Architecture for Carry Select Adder Without Multiplexer

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ABSTRACT
High performance digital adder with less power consumption and reduced area is a fundamental design issues for advanced processors. Carry Select Adder (CSA) is one of the fastest adder used in many processors to perform fast arithmetic function. Many different adder architecture designs have been developed to increase the efficiency of the adder. As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing. Due to which high speed adder and multiplier architecture plays an important role in many applications. In this paper, we proposed a technique for designing of carry select adder without using multiplexer. Verification of CSA architecture is done through design and implementation of 16, 32 and 64 bit. Comparison is done with existing structure of adder and proves the efficiency of our proposed design. These designs are implemented on Xilinx device family.

Keywords
Ripple Carry Adder (RCA), Carry Select Adder (CSA), Binary to Excess-1 converter (BEC).

1. INTRODUCTION
Design of high performance digital adder is an important requirement in advanced digital Signal Processors for fast and accurate computation. The design architecture of high speed and low power VLSI needs efficient arithmetic processing units, which are optimized for the performance parameters i.e. speed and power consumption. Addition is one of the basic fundamental arithmetic operations. Adders are the important components which are commonly found in the many different blocks of microprocessors, microcontrollers and digital signal processing chips. Speed is important criteria for designing of any digital circuits. In digital adders, speed of addition is limited by the time required for a carry to propagate through the adder. In conventional adder the sum for each bit position is generated sequentially only after the previous bit position has been summed and carry propagated into the next position [1]. Carry select adder (CSA) is one of the fastest adder. CSA is used to solve the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the final sum. However, CSA consumes more area because it uses multiple pairs of ripple carry adders(RCA) to generate the partial sum and carry by considering carry input '0' and '1' respectively, then the final sum and carry are chosen by the use of multiplexers [2]. The basic approach used in this paper is to design a CSA without multiplexer so that we can achieve efficient and fast response.

2. BINARY TO EXCESS-1 CONVERTER (BEC)
Binary to excess-1 converter is used to reduce the area and power consumption in Carry Select Adder [3]. Figure 1 shows the basic structure of 4-bit BEC. The Boolean expressions of the 4-bit BEC is as

$X0 = \sim B0$ (1)
$X1 = B0 \wedge B1$ (2)
$X2 = B2 \wedge (B0 \,\&\, B1)$ (3)
$X3 = B3 \wedge (B0 \,\&\, B1 \,\&\, B2)$ (4)

Binary[3:0]	Excess- 1[3:0]
0000	0001
0001	0010
0010	0011
|	|
|	|
|	|
1111	0000

Table 1: Function Table of 4-bit Excess-1 converter (BEC)

The main idea of Binary to excess-1 converter is used instead of the RCA (ripple carry adder) with Cin =1 in order to reduce the area and power consumption of the 16-B Carry Select Adder.

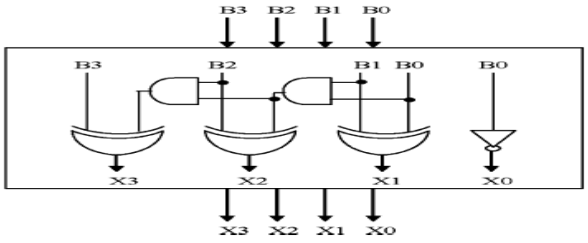

Figure 1: 4-bit Binary to Excess-1 converter (BEC)

3. STRUCTURE OF CONVENTIONAL 16-BIT CARRY SELECT ADDER USING RCA
Figure 2 is the basic structure of the conventional 16-Bit Carry Select Adder. It uses Ripple Carry Adder (RCA). The structure contains five groups with different bit size RCA.

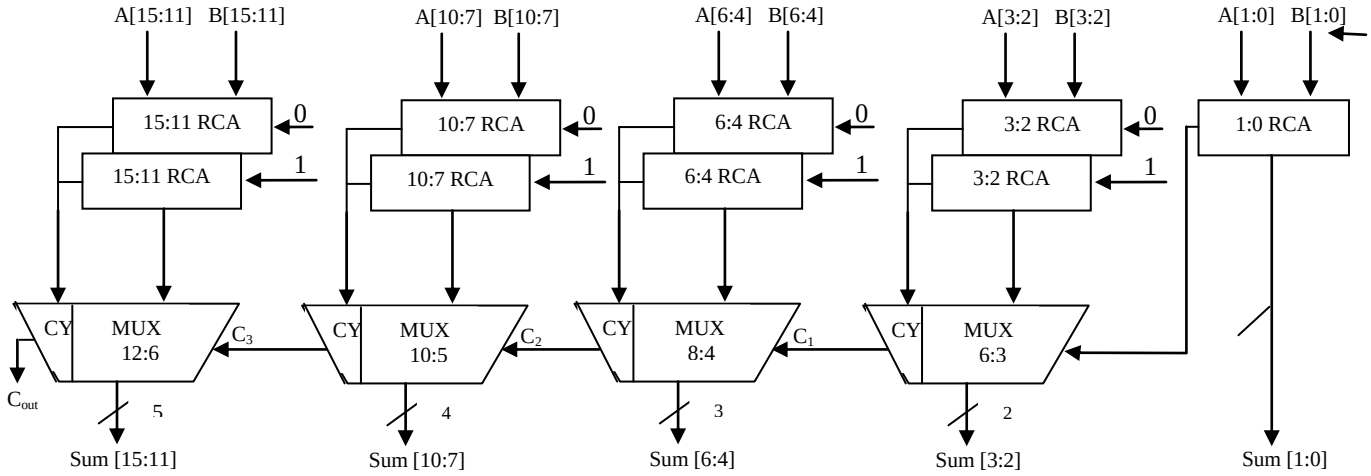

Figure 2: 16-Bit Carry Select Adder using Ripple Carry Adder

The RCA is simplest adder but their performance is limited by a carry that propagate from the lower-significant bit (LSB) to the most-significant bit (MSB). 1st group consist of only one 2-bit RCA which adds the input bits and the carry input and results to sum [1:0] and the carry out. The carry out of the Group 1 which acts as the selection input to mux of group 2. If the carry-in is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is 1, the sum and carry-out of the lower RCA is selected [5]. Similarly the remaining groups will be selected depending on the Cout from the previous groups.

4. PROPOSED MODIFIED STRUCTURE OF 16-B CARRY SELECT ADDER USING BEC

The structure of the modified 16-Bit CSA using BEC is shown in Figure 3. In this architecture instead of the RCA with Ci = 1, BEC block is used.

The structure is again divided into five groups with different bit size RCA and BEC. The Binary to excess-1 Converter (BEC) replaces the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSA [6].

In this structure also group 1 contains only one 2- bit RCA and output of this RCA goes to the next group. From the next group it consist combination of one 2-bit RCA and one 2-bit BEC. One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Multiplexers (mux) is then used to get the final sum and carry .

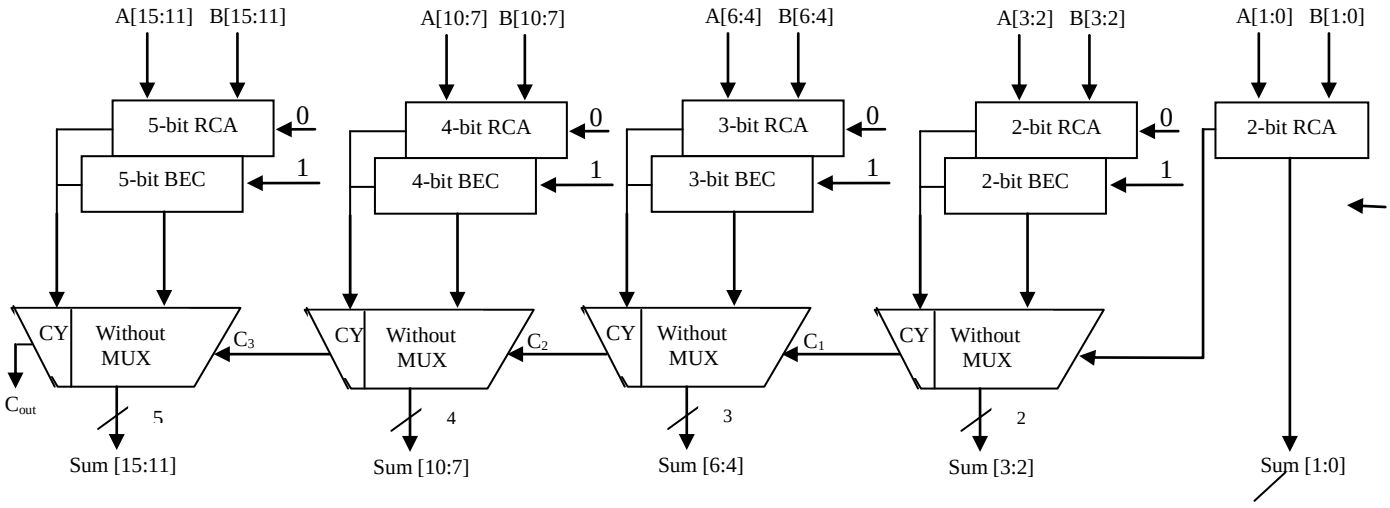

Figure 3: Modified 16-Bit Carry Select Adder using BEC

5. SIMULATION RESULT

In this paper all the designing and experiment regarding algorithm that we have mentioned is being developed on Xilinx 14.3i Spartan 6, Vertex 6 and Vertex 7 updated version family. Xilinx ISE 14.3i provides advanced tools like smart Compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. Xilinx 14.3i has a couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low.

Various adders like regular 16-bit Carry Select Adder using Ripple Carry Adder, proposed 16-bit CSA using RCA and binary to excess one converter (BEC), compressor based multiplier and FIR filter is designed on a Xilinx 14.3i in order to perform comparison. Figure 4 and Figure 5 represents the simulation result of Regular 16-Bit CSA with RCA and proposed modified 16-Bit CSA with BEC respectively.

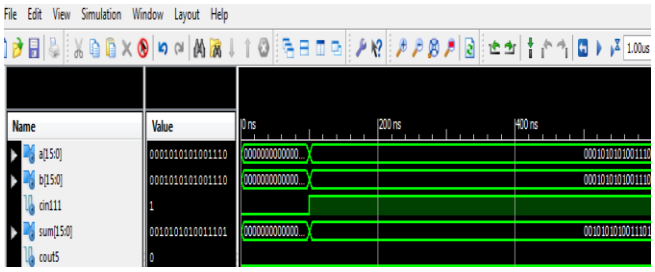

Figure 4: Simulation result of Regular 16-Bit CSA

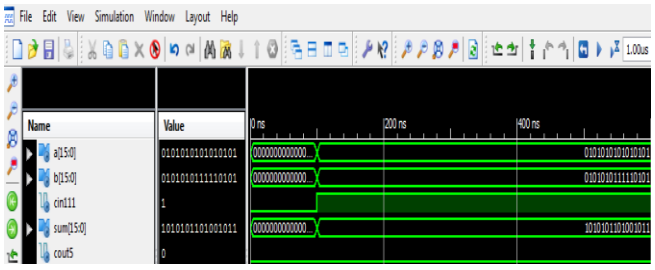

Figure 5: Simulation result of Proposed modified 16-Bit CSA

Table 2: Comparison Table of Adders for Different Device Families

Word size	Adder	Delay(ns) Spartan 6	Delay(ns) Vertex 6	Delay(ns) Vertex 7
16-B CSA	Regular (Dual RCA)	13.292	5.610	4.478
	Modified (With BEC)	11.257	3.933	3.144
32-B CSA	Regular (Dual RCA)	20.733	9.387	7.474
	Modified (With BEC)	17.130	6.948	5.537
64-B CSA	Regular (Dual RCA)	36.599	17.820	14.205
	Modified (With BEC)	28.876	12.977	10.324

Table 2 shows the comparison of adders in different device Table 2 shows the comparison of CSA for different device family and found that the result of our proposed modified CSA is better than conventional CSA among all families.

The comparison graph of regular carry select adder and proposed modified carry select adder in terms of delays for word size 16 is shown in figure 6.

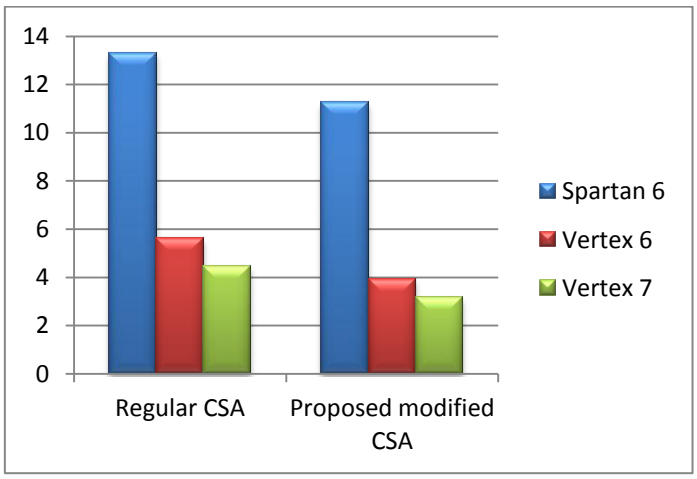

Figure 6: comparison of Adder for Delay (Word Size =16)

Figure 7 shown is the comparison graph for word size 32 for conventional CSA and proposed CSA.

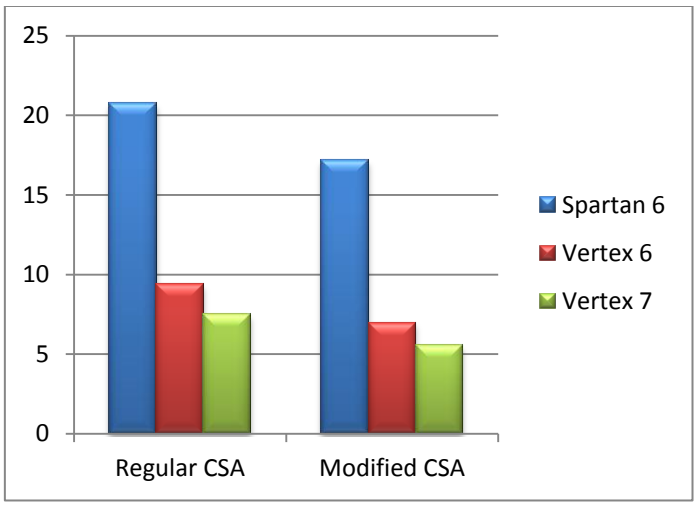

Figure 7: comparison of Adder for Delay (Word Size =32)

Figure 8 shows the comparison of delay for the Carry Select Adder in spartan 6, Vertex 6 and Vertex 7 device family for 64-bit. All the experiment and designing coding have been written in VHDL and the functionality is verified by RTL and gate level simulation.

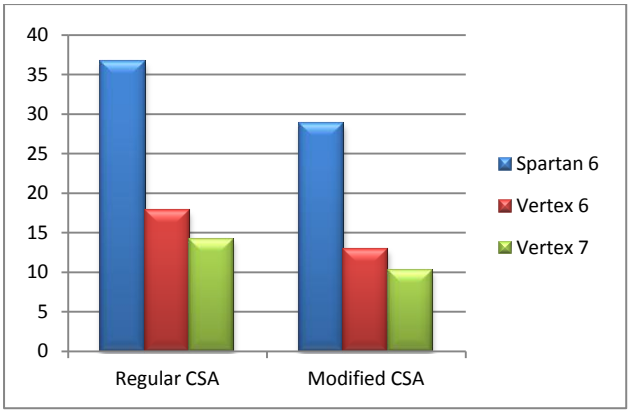

Figure 8: comparison of Adder for Delay (Word Size =64)

6. CONCLUSION

This paper is based on regular and modified carry select adder. Proposed modified Carry Select Adder is a simple technique used in this paper to reduce the delay of Carry Select Adder. In this paper we introduce unique technique i.e. without using multiplexer CSA is implemented and our proposed design improves the performance of system. With the help of this technique one can design an efficient filter. Filter is a combination of adder and multiplier. So in place of simple multiplier you can use effective compressor technique for multiplication process. All the results are synthesized using Xilinx 14.3i software. The regular CSA has a disadvantage of consuming larger area and delay. The modified CSA with BEC and without multiplexer reduces the delay, when compare to conventional CSA. It would be interesting to test the design for higher order bit and for other different device families.

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