Impact of Negative Bias Temperature Instability on 6T CMOS SRAM Cell Performance

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ABSTRACT
This paper presents the effect of negative bias temperature instability (NBTI) on a 6T CMOS SRAM cell and a technique to correct the NBTI induced error. The effect of NBTI on the generation of interface traps and I_{ds}-V_{gs} characteristics is analyzed. The degradation of static noise margin and PMOS transistor's V_{th} with increase in simulation time is analyzed in SRAM cell. Threshold voltage degradation is simulated at two different technologies and it is found that NBTI degradation is prominent in lower technology nodes. As memories occupy the maximum area on a chip, thus, more robust SRAM design is required for high reliability of SRAM cell. MOSFET reliability analysis (MOSRA) model is used to simulate the effects of Bias Temperature Instability and hot carrier injection. Error introduced because of NBTI is corrected using a bit flipping technique.

Keywords
Negative Bias Temperature Instability (NBTI), Static Noise Margin (SNM), SRAM, CMOS, MOSFET.

1. INTRODUCTION
As the technology has evolved, device performance has increased by the scaling of transistor feature sizes which surely has an influence on device reliability. Moving towards lower technology there is reduction in supply voltage which has resulted in increase in electric fields and leakage currents. Scaling results in enhanced power dissipation which leads to performance degradation of the devices. Device characterization in case of higher temperature leads to even more performance degradation. One of the important mechanisms in p-channel metal oxide semiconductor field effect transistor is negative bias temperature instability (NBTI). It occurs because of the application of negative gate source voltage on the PMOS transistor and leads to performance degradation. Infected PMOS transistor in SRAM leads to the degradation of performance and noise margin. SRAM has smaller margin in write ability, timing and cell ability; so more careful design considerations are required. Thus more robust SRAM design is required for high reliability. The effects of NBTI on SRAM have been studied by [1-4]. NBTI causes the threshold voltage to degrade and this effect is accelerated with temperature [5-8]. This paper analyzes a predictive technique to simulate the effect of NBTI using body biasing. Effects of NBTI on SRAM have been studied in detail.

1.1 Mechanism of NBTI
NBTI is a dominant aging mechanism which leads to increase in threshold voltage when a negative gate source voltage V_{gs} is applied on the gate of PMOS transistor as shown in figure 1. It accelerates with increase in temperature [6], [9-10].

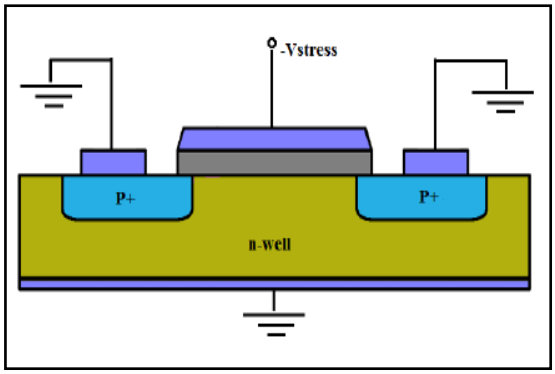

Figure 1 PMOS under NBTI effect [9]

NBTI leads to the generation of interface traps which are formed by the breakdown of Si-H bonds present at the interface of Si-SiO_2. At high temperatures and because of negative bias temperature instability silicon hydrogen bonds at the interface of silicon and silicon dioxide break down thus degrades the parameters like mobility, threshold voltage, delay and trans-conductance.

1.2 Reaction Diffusion Model
It has the capability to reproduce device degradation with time because of negative bias temperature stress. It states that when the PMOS is operating in strong inversion region holes present in the inversion layer reacts with the bonds of Si-H at the interface of Si-SiO2 and thus weakens the bonds. The reaction representing generation of interface traps is represented in equation (1)

$$Si - H + h^{+} \leftrightarrow Si^{*} + H^{0} \qquad (1)$$

The remaing Si^{*} which has a dangling bond acts like a donor interface.The mechanism of Reaction Diffusion model [9-10] is illustrated in figure 2 and 3.

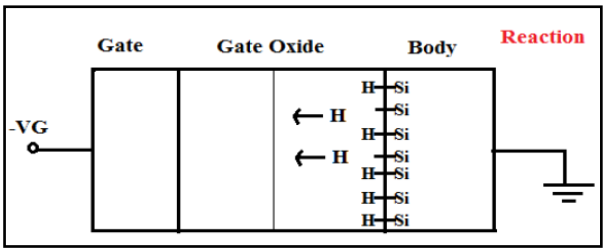

Figure 2: Reaction process [9]

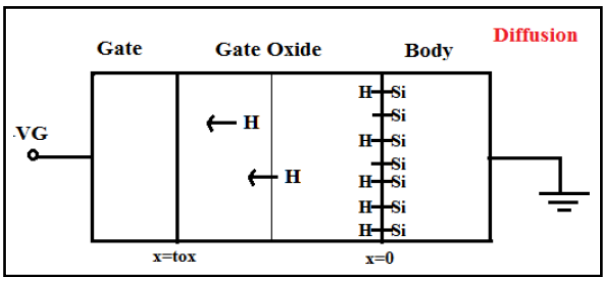

Figure 3 Diffusion process [9]

The produced *H* from the breakdown of the bond diffuse away from the silicon- silicon dioxide interface and thus leads to the formation of interface traps. The rate of interface trap density is given by following equation:

$$\frac{dN_{IT}}{dt} = k_F[N_0 - N_{IT}] - k_R N_{IT} N_H^{(0)} \quad (2)$$

Where, k_F is bond-breaking rate, N_0 is silicon hydrogen bond density, k_R is bond-annealing rate, $N_H^{(0)}$ hydrogen density at the silicon silicon dioxide interface.In this model it is assumed that maximum threshold voltage shift is due to the generation of interface traps. Thus threshold voltage degradation because of interface traps N_{it} is given by the equation

$$\Delta V_t(t) \propto q\Delta N_{it}(t)/C_{ox} \quad (3)$$

Where, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

1.3 Impact of NBTI on PMOS Parameters

Negative bias temperature instability leads to the degradation of following parameters of PMOS transistor:

Threshold Voltage: Threshold voltage is the voltage at which the MOS transistor starts conducting. It is given by following equation.

$$V_{th} = V_{T_0} + \gamma(\sqrt{2\emptyset_B - |V_{sb}|} - \sqrt{2\emptyset_B} + \frac{Q_{it}+Q_{ox}}{C_{ox}} \quad (4)$$

Where,V_{T_0} is the threshold voltage, Q_{ox} is the oxide charge, C_{ox} is the capacitance per unit area, Q_{it} is the interface charge and γ is the body effect parameter defined as

$$\gamma = \frac{\sqrt{2\epsilon_s q_o N_A}}{C_{ox}} \quad (5)$$

Where, $\epsilon_s$defines the permittivity of the silicon substrate and acceptor doping concentration is defined by N_A. $\emptyset_B$ is the potential in neutral p type region given by

$$\emptyset_B = \frac{KT}{q} ln \frac{N_A}{n_i} \quad (6)$$

NBTI leads to the generation of interface and oxide traps which degrades the threshold voltage of the MOS transistor.

Mobility (μ): generation of interface traps leads to the decrease in mobility. According to Devine et al. [8] mobility model

$$\mu = \frac{\mu_o}{1+\propto N_{it}} \quad (7)$$

Drain Current (I_d): Linear Drain Current ($I_{d,lin}$) is given by the following equation:

$$I_{d,lin} = \left(W/l_{eff}\right)\mu_{eff} C_{ox}\left(V_{gs} - V_T - V_{ds}/2\right)(1 + \lambda V_{ds}) \quad (8)$$

Where, λ is the channel length modulation parameter, W is the width of the device, μ_{eff} is the effective mobility and l_{eff} is the effective gate length.

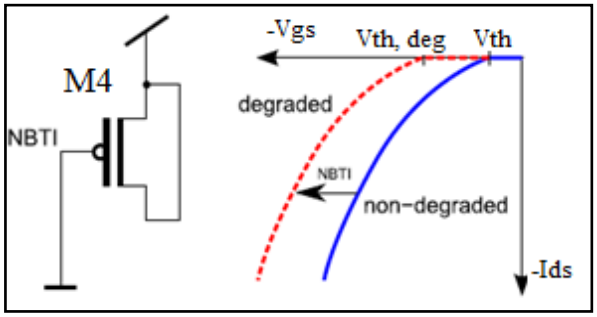

Figure 4 Effect of NBTI on PMOS

Saturation Current ($I_{d,sat}$): drain current in saturation region is given as:

$$I_{d,sat} = (W/2l)\mu_{eff} C_{ox}(V_{gs} - V_T)^2 \quad (9)$$

As the mobility decreases and the threshold voltage increases,the drain current reduces with NBTI stress as shown in Figure 4 and thus leads to performance degradation.

Trans-conductance (g_m):Trans-conductance is the important parameter that gets changed because of NBTI. As the drain current reduces it also decreases according to the following relation.

$$g_m = \frac{\Delta I_d}{\Delta V_g} \quad (10)$$

As the trans-conductance shift model proposed by Devine et al. [8]

$$g_m = g_{m_o} \frac{\propto N_{it}}{1+\propto N_{it}} \quad (11)$$

Where, ∝ is process related parameter and N_{it} is the interface traps.

2. IMPACT OF NBTI ON SRAM PERFORMANCE

Threshold voltage increases because of the effect of NBTI. The change in threshold voltage follows a power law [7-8] as follows:

$$\Delta V_{tp} = K_{dc} \times t^{2.5} \quad (12)$$

Where, K_{dc} is a technology dependent parameter and *t* is time. Figure 5 shows a 6T SRAM cell with two pull up PMOS transistorsP_1 and P_2, two pull down NMOS transistors N_1 and N_3thus making cross coupled inverters and two access transistorsN_2 and N_4. Because of cross coupled inverters when

one PMOS is on the other one is off. Thus one PMOS is always under the stress of NBTI.

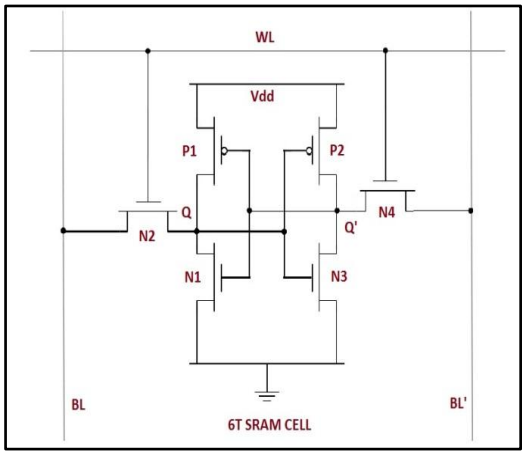

Figure 5 CMOS 6T SRAM cell

SRAM cell works in following three modes

2.1 Standby Mode

During standby mode access transistors are made off because word line is not asserted. Stored data is holded using two cross coupled inverters.

2.2 Write mode

Access transistors are enabled by asserting the word line the data to be written is applied to Bit-line and the inverted data is applied to Bit-bar. Write operation is shown in figure 6.

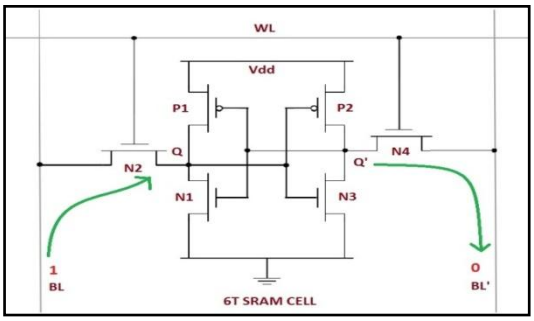

Figure 6 Write operation

2.3 Read mode

Read mode starts by disconnecting the access transistors and pre-charging the bit line and bit line bar to $V_{dd}/2$ and then enabling the access transistors by asserting the word line. Then the node where data *1* is stored starts getting discharged through access transistor to ground and node containing data *0* starts getting charged through access transistor to V_{dd}. Figure 7 shows the read operation**.**

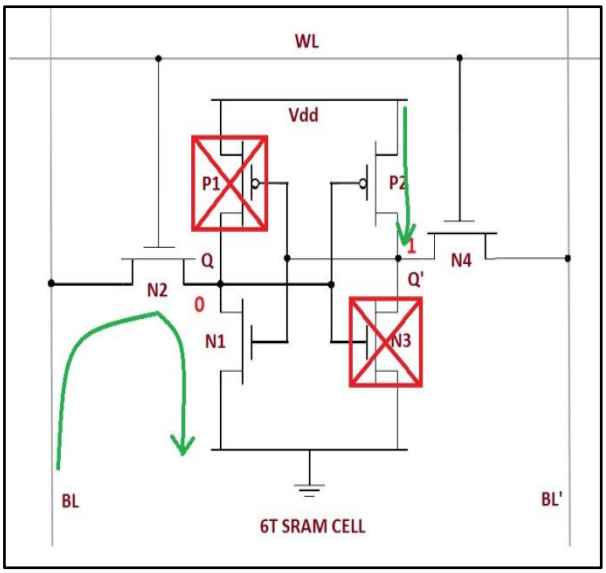

Figure 7 Read operation

Noise margin is the amount of maximum noise which a circuit can tolerate and still performing the correct operation. Figure 8 shows a SNM for a SRAM cell [6]. Reduced static noise margin results in read failure. As because of NBTI trip point of the PMOS decreases because of increase in threshold voltage so under stress conditions static noise margin degrades with aging time. So the cell becomes more susceptible to data flipping during stress conditions.

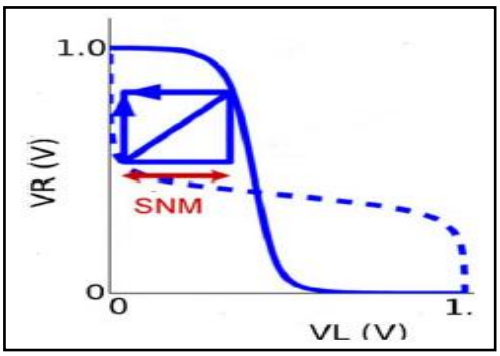

Figure 8 Static noise margin for SRAM [6]

3. SCREENING OF NBTI USING MOSRA

MOSFET Reliability Analysis (MOSRA) is a model used to simulate the effects of Bias Temperature Instability and hot carrier injection. It is used by circuit designers to envisage the reliability of the designs. Reliability analysis consists of simulation in two phases [15].

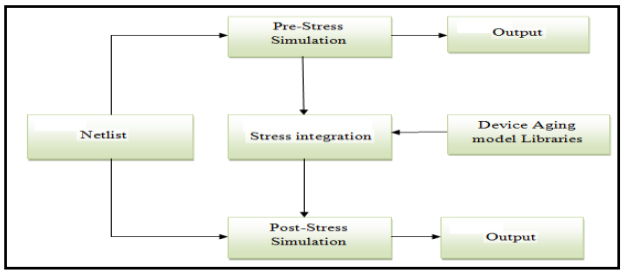

Figure 9 MOSRA flow [15]

3.1 Fresh simulation

It provides the stress information of the MOS transistors based on the circuit behaviour using built-model of NBTI effect in SPICE. The MOSRA equation is integrated over the user specified simulation time in transient analysis to find the stressed value of a parameter. This result is then extrapolated to calculate the final stress after a user specified operation time (age).

3.2 Post-stress simulation

It uses the stress information provided by fresh simulation mode to simulate the degradation effect on the performance of circuit.MOS reliability analysis provides an accurate and efficient method to find the performance degradation of MOS devices with aging. Effects of NBTI have been simulated considering one of the PMOS transistors in SRAM under stress.

4. CORRECTION OF NBTI

The cell works as a regular 6T SRAM cell in the normal mode. An extra transistor *CR* is connected between *Q* and Q_{bar} which controls the mode of working. When *CR* is not connected *Q* and Q_{bar} are disconnected from each other, thus the cell is working in normal mode and performs the regular operations of standby read and write. When the flipping of data is required, control transistor is activated by giving a positive pulse at *CR* thus for that moment both *Q* and Q_{bar} gets connected to each other. Because both of these nodes preserve opposite logic values, the high logic node will start discharging towards ground and the low logic node will starts charging towards V_{dd}. Figure 11 shows the correction circuit for NBTI error [10].

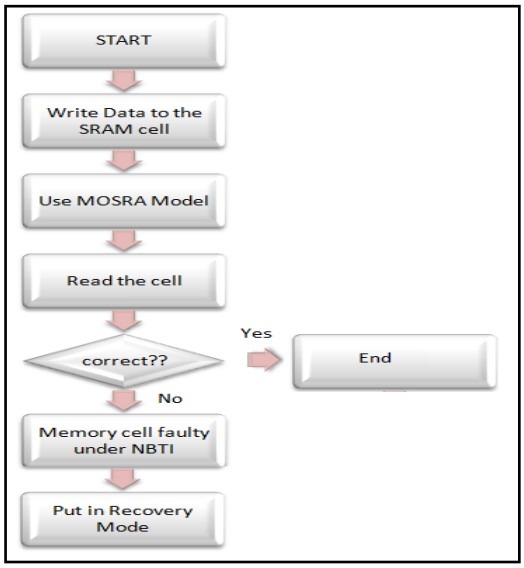

Figure 10 Screening of NBTI effect

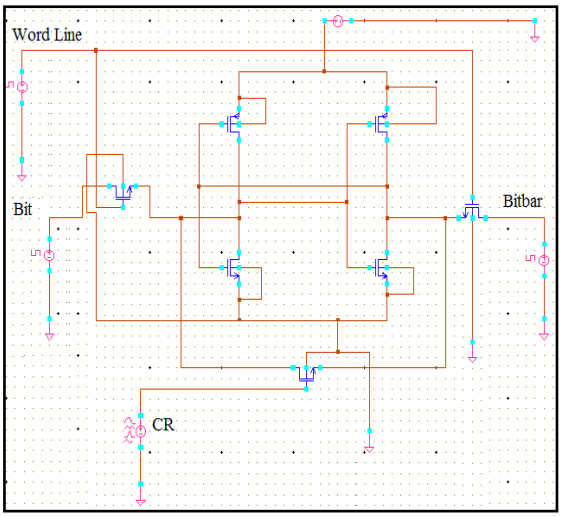

Figure 11 NBTI correction

5. SIMULATION RESULTS

Operation of SRAM cell is shown in figure 12. Word line is enabled for write operation. Bit line is connected to highvoltage and bit bar is connected to low voltage so *Q* will be storing high logic and Q_{bar}will be storing low logic. Read operation is initiated by disabling the word line and pre-charging the bit line and bit bar line to $V_{dd}/2$. After the pre-charging is done word line is enabled. As *Q* node was storing logic 1 thus bit line will start getting charged and bit bar will start getting discharged, when the sense amplifier is enabled bit line gets fully charged to V_{dd} thus reading 1 and similarly bit bar gets fully discharged to ground and thus reading logic 0.

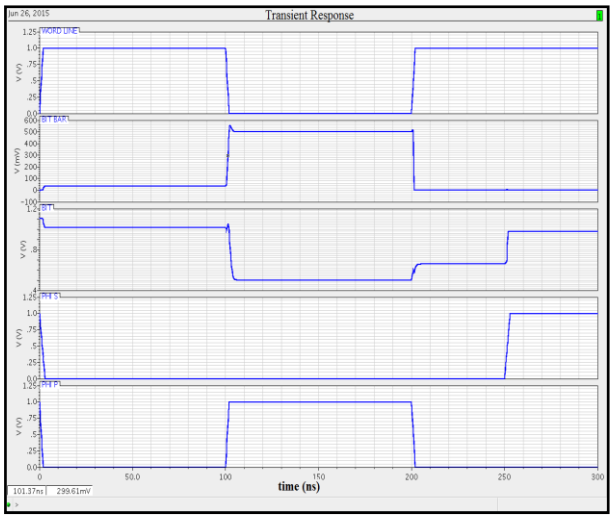

Figure 12 SRAM read and write operation

5.1 Shift in I_d-V_{gs} characteristics

NBTI leads to increase in threshold voltage of PMOS transistor. The change in I_d-V_{gs} characteristics of a PMOS is analyzed using reaction diffusion model is shown in figure 13.

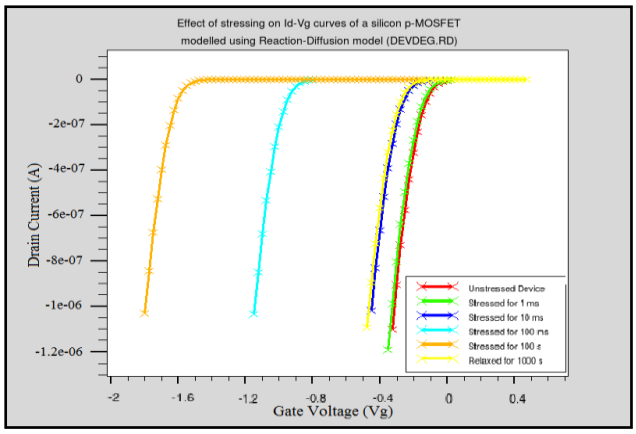

Figure 13 I_d-V_{gs} characteristics of PMOS for different stress times

5.2 Shift in threshold voltage

The swing in threshold voltage with time up to 10^{10} seconds has been analyzed at 32 nm and 45 nm technology using MOSRA model in SPICE. It can be seen from figure 14 that threshold voltage degradation is more prominent in case of 32nm technology node.

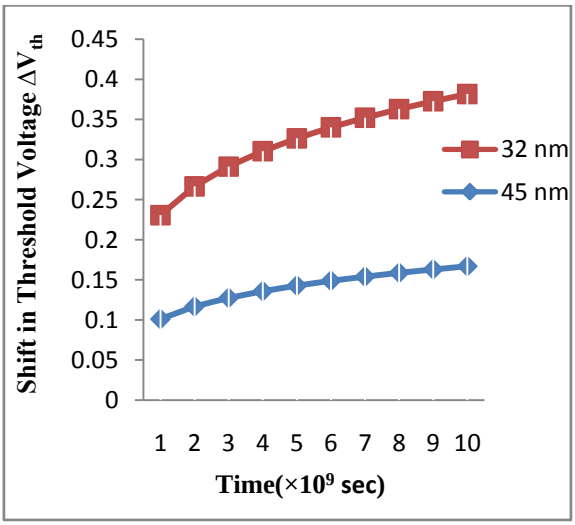

Figure 14 Threshold Vs time for 32nm and 45nm technology nodes

Table 1 Percentage increase in threshold voltage

Technology node	Percentage average increase in threshold voltage (V_{th})
45nm	28%
32nm	37%

Percentage average change in threshold voltage at 45nm and 32nm technology is listed in Table 1.

5 Static Noise Margin

The figure 15 and 16 show signal to noise margin graph for SRAM before and after the effect of NBTI. Table 2 gives the value of threshold voltage degradation with time.

Table 2 Threshold voltage degradation with time

Time(seconds)	SNM
0	0.4152
1×10^9	0.3702
2×10^9	0.3667
3×10^9	0.3630
4×10^9	0.3608
5×10^9	0.3584
6×10^9	0.3561
7×10^9	0.3538
8×10^9	0.3518
9×10^9	0.3496
10×10^9	0.3480

It can be seen that with increase in threshold voltage static noise margin has decreased.

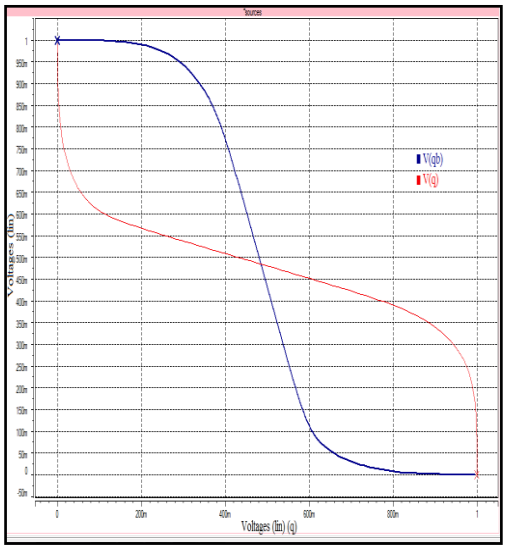

Figure 15 Butterfly curve before NBTI effect

5.4 Correcting the NBTI Error

In figure 17 node Q is storing *1* initially and Q_{bar} is storing *0* when these both nodes are connected for a certain time Q will get discharged to ground and Q_{bar} will get charged to V_{dd}. Time for which pulse is given at *CR* depends on the time taken by the node Q to discharge to a value such that it start acting as logic *0* and similarly for the node Q_{bar} to charge to a value such that it start acting as logic 1. Pulse width of the flip pulse used here is 480 ps to correct the error. When the pulse is removed from *CR*, Q holds a new logic *0* and Q_{bar} logic *1*.

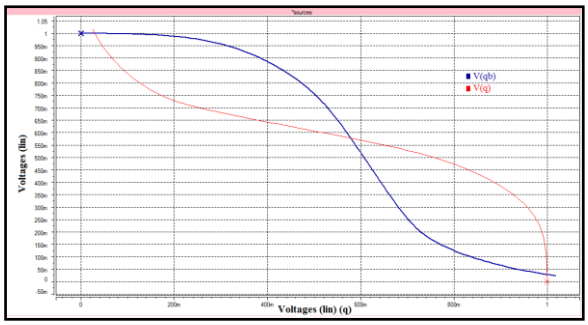

Figure 16 Butterfly curve after NBTI effect

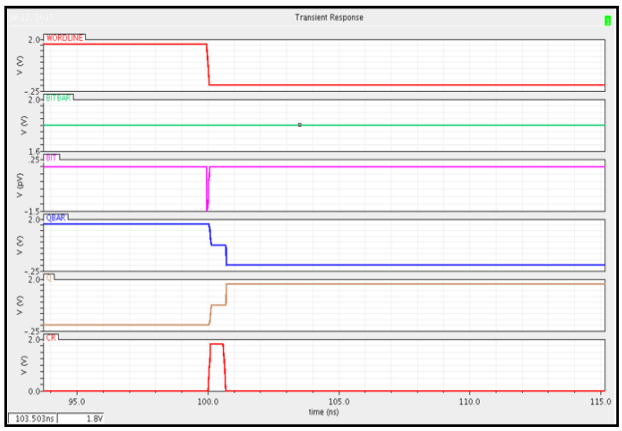

Figure 17 NBTI error correction

6. CONCLUSION

Negative bias temperature instability is an aging effect which impacts the performance of PMOS transistors. A normal applied negative voltage at the gate of PMOS transistor leads to the generation of interface traps at the Si/SiO_2 interface. These interface traps leads to increase in threshold voltage thus degrading the performance of the PMOS transistors. This paper presents a method to simulate the NBTI effect on SRAM using MOSRA model. MOSRA is an efficient and accurate method to simulate the aging effects in devices. Effects of NBTI on SRAM static noise margin have been analyzed. Static noise margin decrease with simulation time because threshold voltage decreases with time due to aging. It has been seen that SNM decreases by approx. 16% after 10^{10} seconds. Change in threshold voltage has been analyzed at 32nm and 45 nm technologies and it has been found that at 32nm the threshold voltage degradation is more than 45nm. At 45 nm technologyThreshold voltage increases by approx. 28% after 10^{10} seconds and at 32 nm this increase is approx. 37%. A technique by flipping the data in SRAM cell to correct NBTI induced error has also discussed.

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