Design and Simulation of Convolutional Viterbi Decoder with Rate-1/3 for MIMO-OFDM System

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ABSTRACT
The errors caused in the wireless communication channel are very important to identify and rectify. Viterbi Decoder is very commonly implemented technique among the various error detection and correction (EDAC) techniques. A high data-rate convolutional code suffers from decrease in the performance of bit-error-rate due to inherent drifting error between the estimated and the accurate path matric and the optimal path matric calculation during the trellis generation. The design performance is highly dependent on many factors like availability of memory elements, decoding latency of the circuit, overhead bits in the algorithm, etc. In this paper, we propose a design of Convolutional Viterbi Rate-1/3 Encoder and Decoder for a wireless communication system based on IEEE 802.11n Draft. The proposed work focuses on high data rate decoder design and simulation. The transmitter encoder and the receiver decoder are designed and simulated as separate designs for functionality verification. The purpose is to determine the feasibility to design data Error Detection And Correction (EDAC) decoder for a wireless system with multiple input multiple output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM). Viterbi Encoder/Decoder combination is very effectively used in high data rate communication systems because of its EDAC feature. The operational concept of viterbi encoding and decoding is based on Trellis coded modulation and de-modulation.

General Terms
Trace Back, Viterbi Decoder, Xilinx, Wireless Communication System.

Keywords
Convolution Code, EDAC, Encoder Rate, MIMO System, OFDM.

1. INTRODUCTION
In high data rate wireless communication, orthogonal frequency division multiplexing is effectively used in many of the present LAN based systems. In wireless networks the most important task is to set-up a data communication link between two nodes (transmitter and receiver) with NO-error or with minimum correctable errors. A MIMO based communication the system provides a feature to reduce the errors with the help of system architecture. An error detection and correction based technique implementation in the system helps to remove the received errors that gets introduced in the data via wireless communication environment. Researchers have proposed many EDAC methods with their efficiencies and implementation features. The selection of an efficient EDAC implementation for a particular communication system is based on various factors like intensity of noise in the channel, speed of communication system hardware, type of communication network, etc. The University of Hawaii introduced the first wireless system ALOHA net. Later two standards for wireless system were developed: IEEE 802.11 and HIPERLAN. However HIPERLAN does not received a success in commercial market. In [1]-[2] the authors has shown design of a wireless communication system. An overview of MIMO-OFDM implementation is shown in [3]-[4]. The performance analysis of MIMO OFDM based wireless system is shown in [5]-[8]. A review on wireless communication system implementation is given by the authors in [9]-[10]. An FPGA based design of OFDM system is given in [11]-[14]. The convolution encoding and decoding based Viterbi Decoder design and implementation is shown in references [15]-[18]. In the proposed paper, section-II elaborates the Transmitter and Receiver sections of MIMO-OFDM based communication system. Section-III elaborates convolutional Viterbi Encoder and Decoder architectures. Section-IV gives simulation result of the Encoder and Decoder designs. The conclusion of the proposed work is summarized in Section-V. At last, the references are mentioned.

2. MIMO-OFDM ARCHITECTURE
Orthogonal Frequency Division Multiplexing is a multi-carrier modulation technique which is very popular in wireless communication networks for data transmission and reception. In OFDM, radio frequency carrier signal are used for wireless signal communication. A simple block diagram of OFDM based system is shown in Fig-1. In such a system, as shown in Fig-1, the data that contains the information is encoded using a convolutional coding technique, preferably error detection and correction coding technique. This stage is the most important unit of such a system. The accuracy of the received data to the actual transmitted information, improves directly in proportion to the error correction efficiency of the convolutional decoder. In the communication system, data interleaving is performed on the encoded data. In the interleaving process, the encoded data is first arranged in matrix and then the rows and columns are interchanged. The interleaving/de-interleaving helps the recovery of data affected by burst error by performing uniform error-distribution in the received data stream. In the transmitter section, the data bits from the interleaved data stream are further grouped to map with the complex numbers representing the OFDM modulation type. Each mapped group of bits is then represented by a number that further represents a particular sub-carrier phase and frequency according to the type of the Quadrature Phase Shift Keying (QPSK).

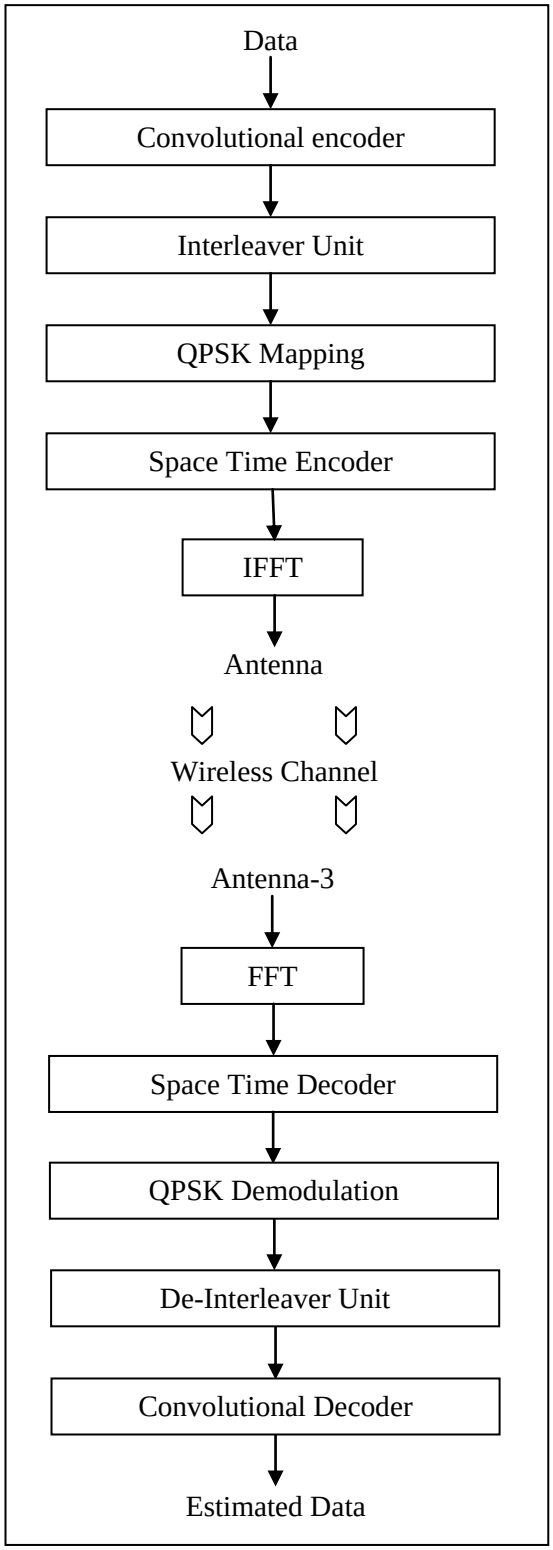

Fig 1:Single Channel OFDM Communication

QPSK modulated data is ready to be transmitted through the communication channel after space-time encoding. At the receiver end, the received data is space-time decoded. Then QPSK demodulation is performed to get the estimated interleaved data stream. The QPSK demodulation output is a bit stream that is related to the received signal corresponding to a particular phase and frequency. This data stream is operated by De-interleaver and then convolutional decoding is performed to obtain the estimated data.

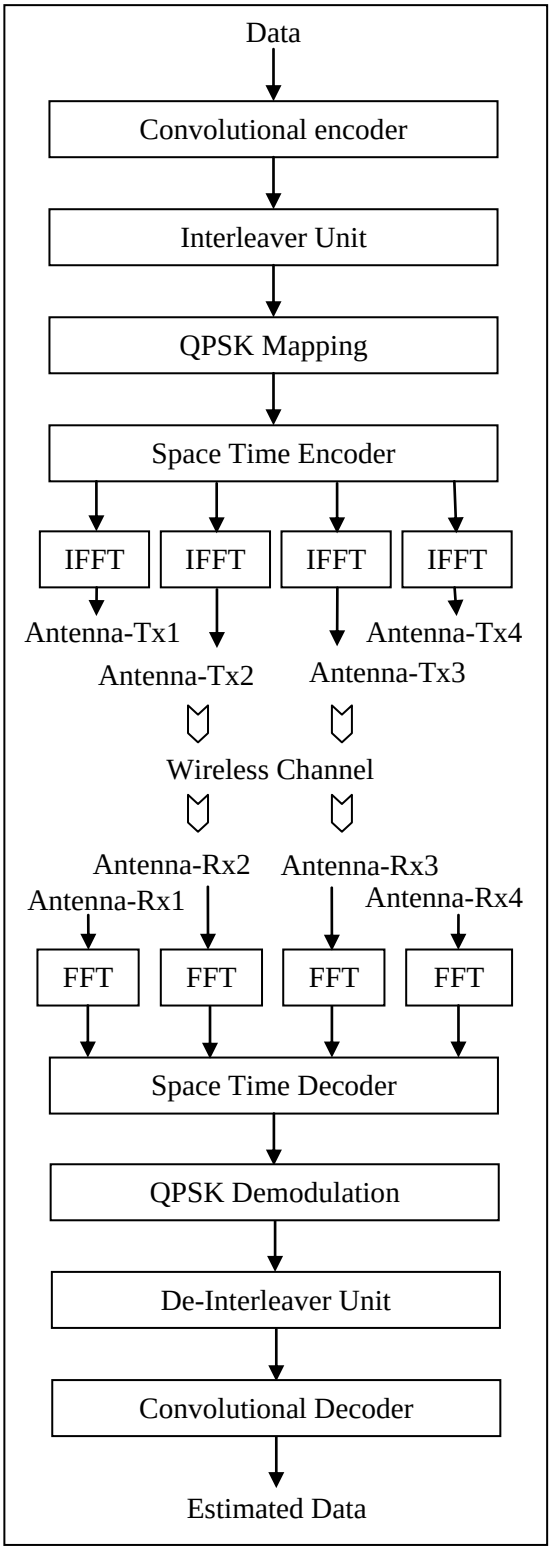

Fig2:MIMO OFDM Communication

In a multiple-input-multiple-output channel based OFDM communication system, as shown in Fig-2, the transmitter section uses multiple antennas to transmit the QPSK modulated data at different frequencies in the wireless channel. At the receiver end, the signals from each receiver-antenna are processed parallel to get the transmitted data. This data is then QPSK demodulates. When a complete set of bit stream corresponding to data-packet size is received then de-interleaving of these bits is performed. The de-interleaved

data bits are de-coded using convolutional decoder. A serial decoding is thus performed on encoded symbol bits. The convolutional decoder provides the estimated data as the output.

3. VITERBI ENCODER-DECODER DESIGN

The encoder and decoder implementation plays a very important role in wireless communication. A number of encoder/decoder designs are proposed by researchers. Viterbi encoder/decoder algorithm implementation in communication system offers two main benefits: (i) encoding of data that improves security of data by unauthorized users, and (ii) error correction in the received data. The combination of these features makes viterbi encoder/decoder a very good option for its implementation. The viterbi encoder is a convolutional encoder. In the encoder, each serially incoming symbol is encoded with a specific number of output bit stream. The ratio of the number of data bits in the input to the number of bits in the output defines the rate of the encoder. For example, a rate=1/3 encoder has 3-bits as encoded output for every serially incoming bit, and for a rate=3/4 encoder has 4-bits as encoded output for every serially 3-bit input. An encoder with 'p' number of input bits and 'q' number of corresponding encoded bits is called as rate "p/q" encoder. The encoder output is a combination of current input data and the state of the encoder register. A continuous sequence of maximum of four input '0'-bit will drive all the encoder registers and the encoded output bits to logic-'0' state. This is also the initial state of the encoder. The minimum '0'-bit at the input that is required to drive the encoder to initial state depends on the present state of the encoder registers. The length of the encoder is the number of flip-flops or memory elements that are used in the encoder serial shift-register. In the present work, rate=1/3 viterbi encoder is simulated that has 4-flipflops in the encoder shift-register. The output logic generation is shown in Fig-3.

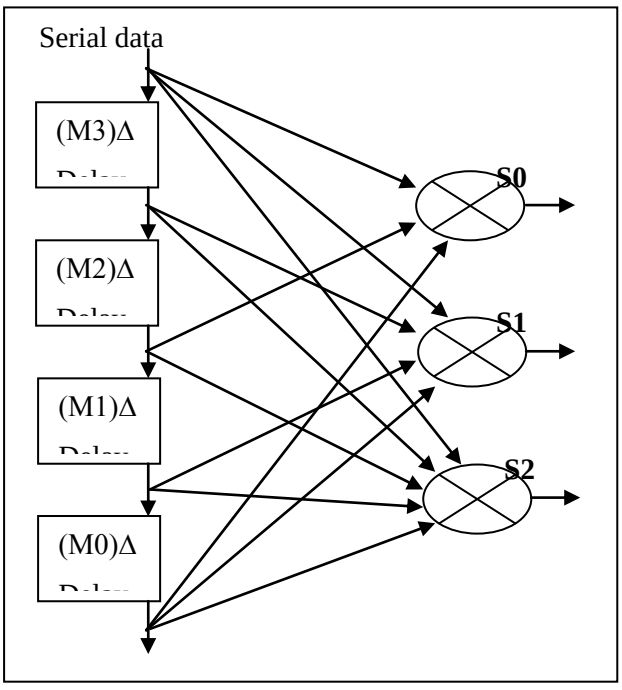

Fig 3: Viterbi Encoder output logic diagram

In the Encoder, the output logics S0, S1 and S2 are generated using the memory state and input logic and it can be represented using following equations:

S0 = S_inxor M2 xor M0 … (i)

S1 = S_inxor M3 xor M1 xor M0 … (ii)

S2 = S_inxor M3 xor M2 xor M1 xor M0 … (iii)

Where, S_in is the serial input data bit, M0 M1, M2, M3 are states of the memory elements.

The decoding steps of the viterbi decoder are shown in Fig-4 with the help of a simple block flow diagram. The serially received data is processed to compute branch metric and path metric. The metric computation is based on the difference of number of bits values in the received data bits and the expected bits. The estimated data is considered by back-trace processing of data bits on the path with minimum path metric value, i.e., the path that shows minimum bit change during decoding process.

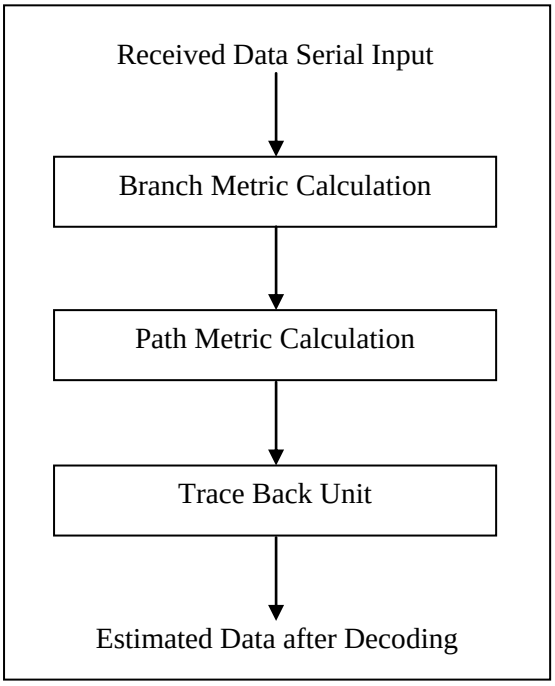

Fig 4: Viterbi Decoder Simple Block diagram

4. SIMULATION RESULTS

The present work is simulated using Xilinx. The block diagrams and the RTL Schematic of proposed Encoder and Decoder designs are shown in Fig-5, Fig-6, Fig-7 and Fig-8 respectively.

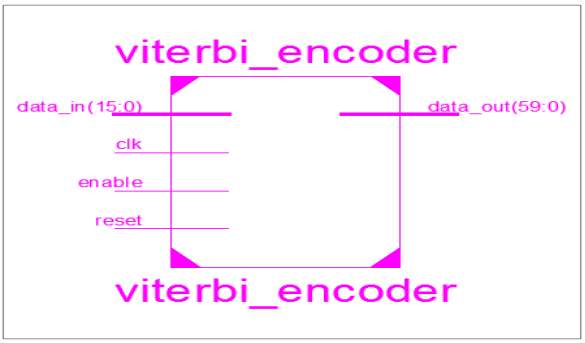

Fig 5: Block Diagram of Proposed Encoder

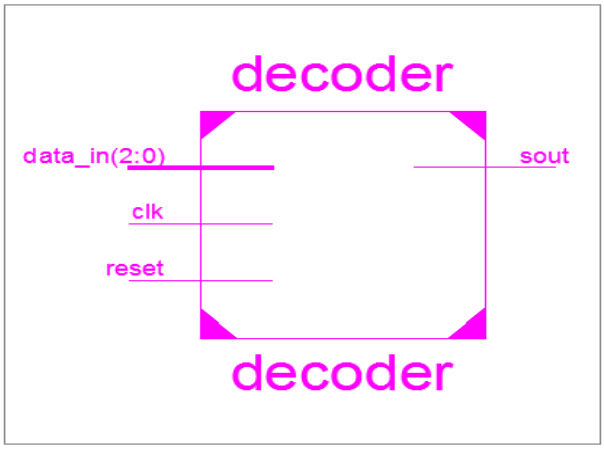

Fig 6: Block Diagram of Proposed Decoder

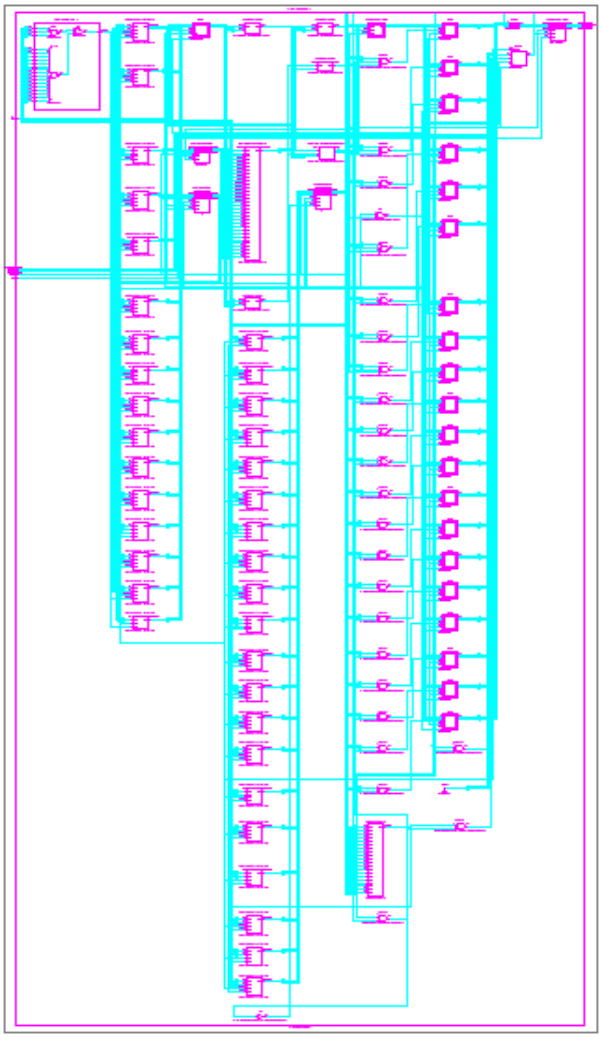

Fig 7: RTL Schematic of Proposed Encoder on Xilinx

The Hardware Utilization summary is presented in Table-1. The operational clock frequency vs dynamic power consumption summary of the proposed design is shown in Table-2.

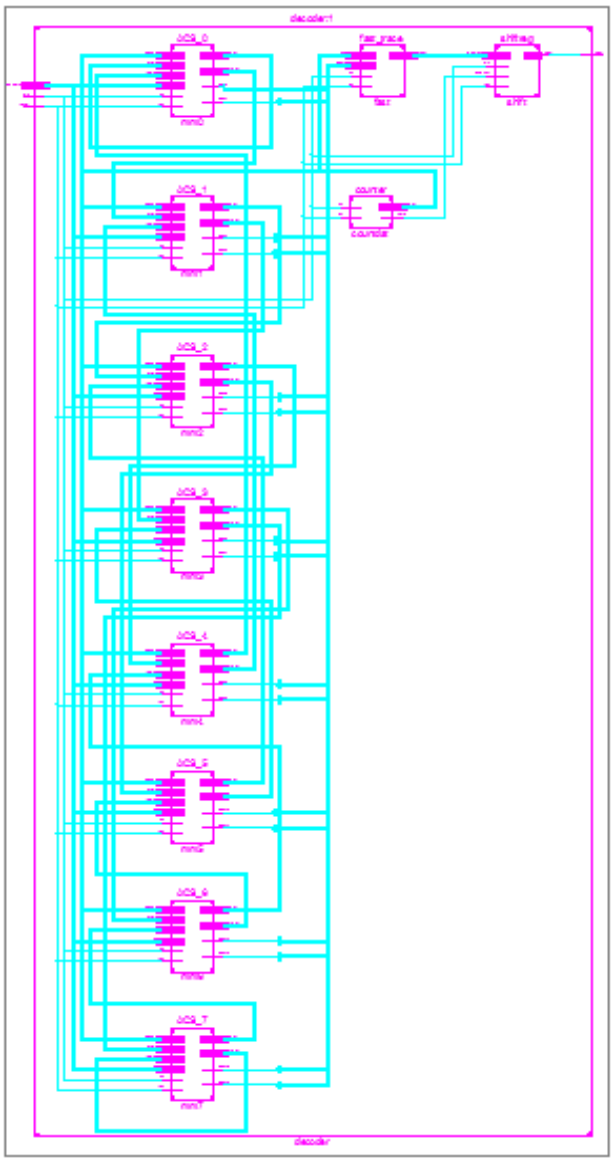

Fig 8: RTL Schematic of Proposed Decoder on Xilinx

Table 1. Table captions should be placed above the table

Spartan-3E XC3S500E-4PQ208	Total	Encoder		Decoder	
		Used	%	Used	%
Slices	4656	153	3	437	9
Flipflops	9312	101	1	362	3
LUTs	9312	202	2	609	6

Table 2. Table captions should be placed above the table

Device	Frequency (MHz)	Dynamic Power Consumption (W)	
		Encoder	Decoder
Spartan-3E XC3S500E -4PQ208	1200	0.060	0.226
	1000	0.050	0.192
	800	0.040	0.157
	500	0.025	0.099

A 16-bit data is used to encode using the proposed encoder. The input data bits are followed by logic-'0' inputs. Following are the input and output simulation data:

Example-1: simulation without error in transmitted data

Input 16-bit – 1011011001101101
Encoder Output (Binary) – 111 110 010 111 100 100 000 100 011 110 110 011 100 000 100 100 111 010 110 111
Encoder Output (Octal) – 76274404366340447267

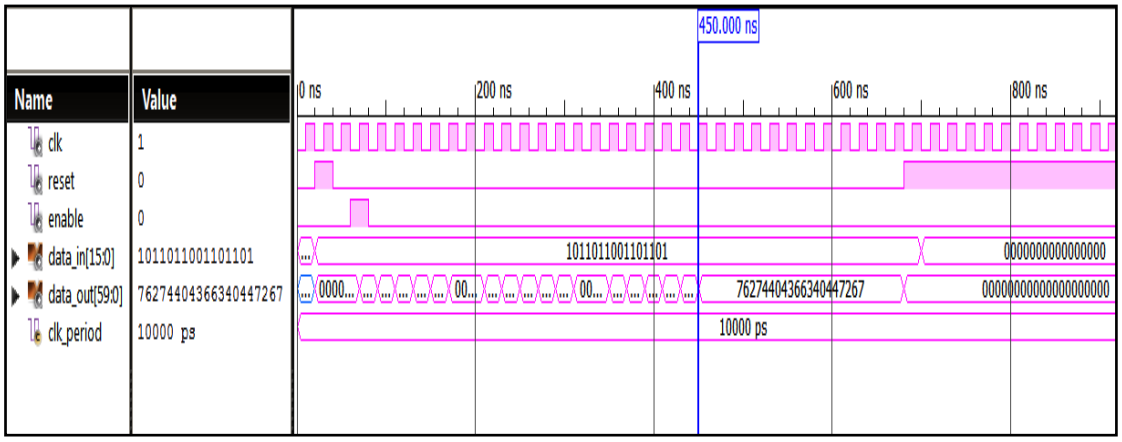

Fig 9: Simulation Waveform of Proposed Encoder

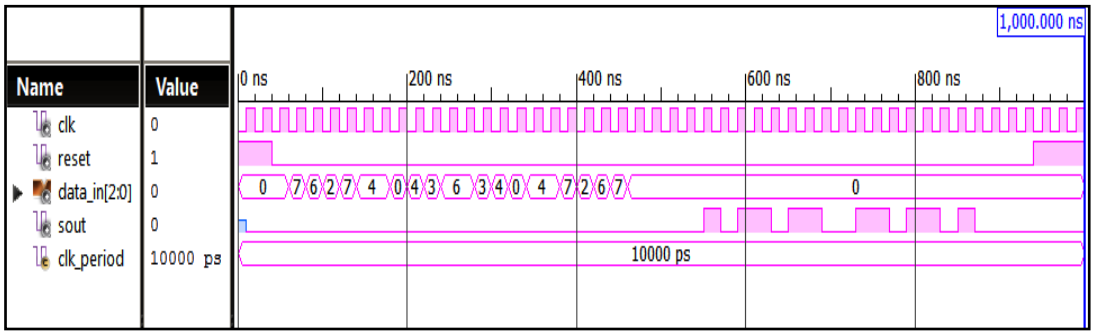

Fig 10: Simulation Waveform of Proposed Decoder

5. CONCLUSION

A Viterbi Decoder is very effective design to detect and correct errors in wireless communication. The limit of number of error bits that can be corrected by a particular algorithm using Viterbi concept is very much dependent on the allowable complexity of the implementation algorithm. A rate-1/3 Viterbi Encoder is an effective algorithm to detect and correct single bit error in a transmitted symbol.

Example-2: simulation with error in transmitted data and error-correction by decoder

Input 16-bit – 1011011001101101

Encoder Output (Binary) – 111 110 010 111 100 100 0**1**0 100 011 110 **00**0 011 100 000 100 100 111 010 11**1** 111

Encoder Output (Octal) – 76274404366340447267

Encoder and Decoder simulation waveforms are shown in Fig-9 and Fig-10 respectively.

The proposed work shows a design simulation of rate-1/3 viterbi encoder / decoder for a wireless communication system that is based on multiple-input-multiple-output OFDM. The proposed concept can be introduced effectively with large sized data while maintaining the same error identification and correction ability of the design

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