

Reversible Logic Synthesis of Sequential Circuits

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ABSTRACT

Reversible logic is gaining importance in recent years largely due to its property of low power consumption. It has a wide range of applications which include advance computing, low power CMOS, optical information processing, quantum computing, DNA cryptography and nanotechnology. Reversible gates are the building blocks of quantum computation. This paper presents a novel design of D, JK and T flip-flops using the existing reversible gates. All circuits have been modeled and verified using Verilog and Modelsim. A comparative study in terms of the number of gates, number of garbage outputs and quantum costs is also presented.

General Terms

Reversible logic, Quantum Cost, Reversible Gates, Sequential Circuits.

Keywords

Reversible logic, Power consumption, CMOS, Nanotechnology, Reversible gates, Flip-flops, Garbage Output.

1. INTRODUCTION

As Moore's law continues to hold, miniaturization of integrated chips continues to take place. This leads to more power dissipation. Cumulative reduction of chip size will eventually lead to quantum dimensional components. Conventional logic circuits dissipate heat energy during their operations. These circuits perform irreversible computations which results in loss of information and it was shown by Landauer that this information loss dissipates $kT \ln 2$ amount of heat. On further investigation Bennet[1] showed that information is lost when the input vector cannot be uniquely recovered from its output vectors and the energy dissipated is directly linked with the number of bits lost. Heat dissipation can be prevented if reversible circuits are used. Information loss can be prevented if the input bits can be completely recovered from the output. Hence the property of reversibility[1][2], will be an important aspect in future circuit design and it is important to realize technology that is capable of operating at such atomic levels while following the property of reversibility to ensure low power dissipation.

However, reversible logic[4][5][6][7] is suffering from two problems. Firstly, there is a shortage of technology with which reversible gates[8][9] can be built. Work is continuing in this field. Secondly, though a lot of research is being done on how to design combinational circuits using reversible logic, very few work is being done in the area of sequential reversible logic implementations[10][11][12][13][14][15]. There is no limitation inherent to reversible logic preventing the design of sequential circuits; in fact when Tommaso Toffoli first characterized reversible logic in his 1980 work 'Reversible Computing' he stated that "Using invertible logic

gates, it is ideally possible to build a sequential computer with zero internal power dissipation".

1.1 Reversible Logic Synthesis

A reversible circuit[8][9] is a circuit in which the number of output vectors is equal to the number of input vectors and there is a one to one mapping between each input and output vector. For example let an input vector I_V and an output vector O_V be defined as follows:

$$I_V = (I_1; I_2; I_3; I_i; \dots; I_n)$$
$$O_V = (O_1; O_2; O_3; O_i; \dots; O_n)$$

Then $I_j \leftrightarrow O_j$, $\forall j$ and $j=1,2,3,i,\dots,n$

1.1.1 Cost Metrics

The cost metrics in logic circuits include the quantum cost, delay and the number of garbage outputs.

1.1.2 Quantum Cost

The quantum cost of circuit is defined in terms of the number of primitive gates used.

1.1.3 Garbage Output

The number of unused or unwanted outputs which are obtained to satisfy the condition of reversibility is called the garbage output.

2. BASIC QUANTUM GATES

2.1 Feynman Gate

Also known as the Controlled NOT Gate or CNOT Gate[8][9], this gate is a multi-qubit gate and also one of the most important quantum gates. Any quantum circuit can be implemented using only this gate and this gate is considered the universal gate for a quantum circuit. It consists of a control and target qubit and changes the value of the target depending on the value of the control. The quantum cost of CNOT Gate is 1. Two input vectors A and B are mapped to the corresponding output vectors P and Q. Here, the input A is the control which determines whether the target input B is to be complemented or not through the XOR operation.

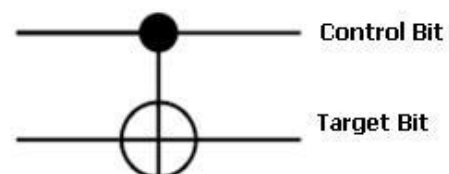


Fig 1: CNOT Circuit

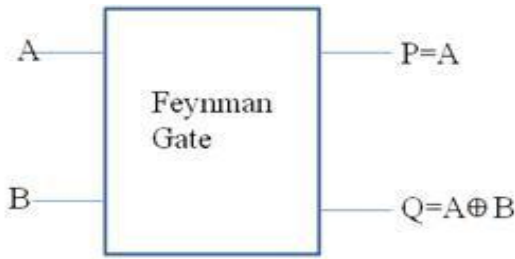


Fig 2: CNOT: Block Diagram

The Double Feynman Gate is similar to the Feynman Gate in operation but has an extra input vector. Correspondingly the quantum cost is 2. The block diagram of Double Feynman gate is shown below.

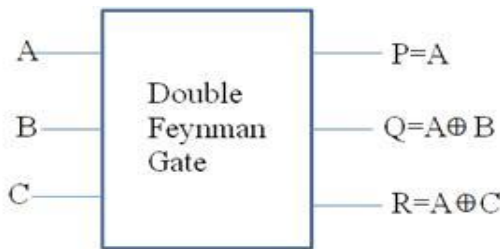


Fig 3: Double Feynman Gate

2.2 Toffoli Gate

The Toffoli Gate has a quantum cost of 5. The relation between the input vector I(A,B,C) and output vector O(P,Q,R) is shown in the figure below. The AND and NAND operations can be realized using this gate and hence any classical circuit can be implemented using this gate.



Fig 4: Toffoli Block Diagram

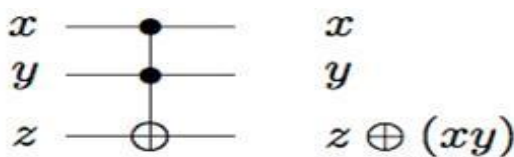


Fig 5: Toffoli Circuit Diagram

2.3 Fredkin Gate

Similar to the Toffoli gate, it has a quantum cost of 5 and the input and output vectors I(A, B, C) and O(P, Q, R) are related as shown in the figure below.

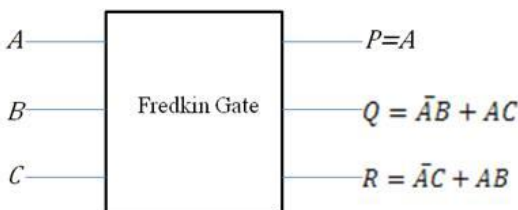


Fig 6: Fredkin Gate Block Diagram

The Fredkin gate[8] can be used to swap the inputs at the output or to perform the if-else condition. In the above figure, if the value of A=1, we get Q=C and R=B. Hence the inputs get swapped at the output. There is also a 4-input Fredkin gate, whose block diagram is shown below. The quantum cost of the 4 input Fredkin Gate is 5.

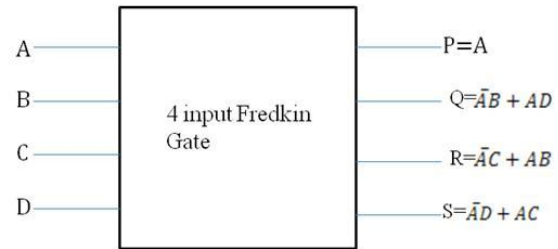


Fig 7: Block Diagram of 4-Input Fredkin Gate

2.4 Peres Gate

The Peres Gate[8] incorporates the functions of both the CNOT and the Toffoli gate and is therefore useful for a large number of quantum operations. The Quantum Cost of Peres Gate is 4.

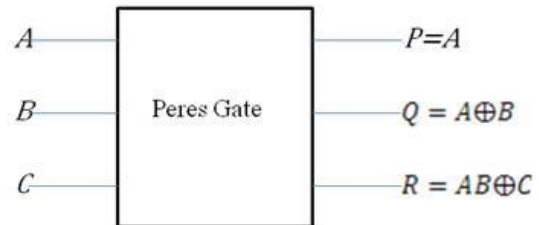


Fig 8: Block Diagram of Peres Gate

The Pauli-X gate[8] acts on a single qubit. It is the quantum equivalent of a NOT gate (with respect to the standard basis $|0\rangle, |1\rangle$, which privileges the Z-direction)

It equates to a rotation of the Bloch Sphere around the X-axis by π radians. It maps $|0\rangle$ to $|1\rangle$ and $|1\rangle$ to $|0\rangle$. It is represented by the Pauli matrix:

$$X = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$$

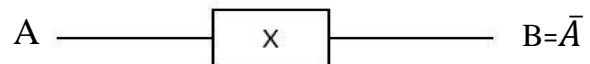


Fig 9: Block Diagram of NOT Gate

3. RELATED WORKS

Thapliyal[3] proposed a circuit of D Flip Flop using seven reversible gates with eight garbage outputs. The circuit is shown in figure 10.

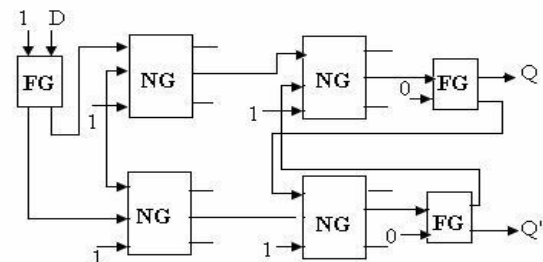


Fig 10: Reversible D Flip Flop with 7 gates

Ali[9] proposed an improved version of Thapliyal’s reversible D Flip Flop which was a realization of the conventional D Flip Flop sequential circuit. Ali proposed a new gate, BME gate which was used to optimize the existing reversible circuit based on the number of reversible gates used and the garbage outputs produced. The number of gates was reduced to four and the number of garbage outputs was also reduced to four. A RS Flip Flop was used for the implementation of this circuit. The optimized circuit is shown below.

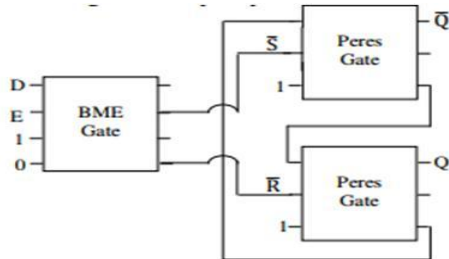


Fig 11: Reversible D Flip Flop with 3 Gates

Thapliyal[3] also proposed circuits of JK and T Flip Flops. The circuits are shown in figures 12 and 13 respectively. Both the circuits are designed using ten reversible gates and the garbage outputs of both the circuits is twelve.

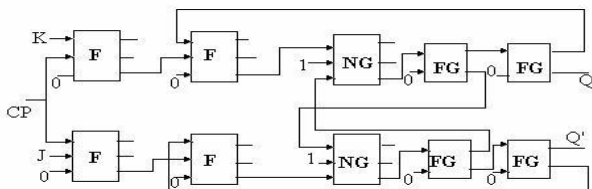


Fig 12: Reversible JK Flip Flop

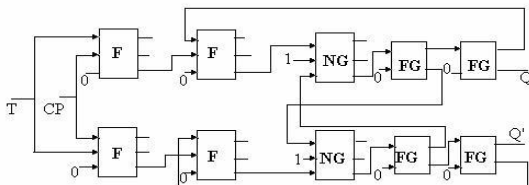


Fig 13: Reversible T Flip Flop

4. PROPOSED METHOD

The logical expression of D flip flop can be reduced to

$$Q(t + 1) = \overline{CLK}.Q(t) + CLK.D$$

In reversible logic, the D flip flop can be implemented by using just one 4-input Fredkin gate. By making the third input 0, the above equation can be obtained, as shown in the figure below.

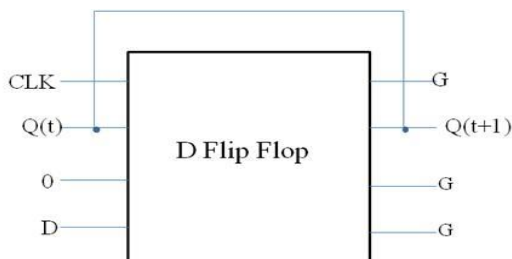


Fig 14: Proposed D Flip Flop using Reversible Gates

Similarly, the derived equation of JK flip flop is given by

$$Q(t + 1) = \overline{CLK}.Q(t) + CLK(J.\overline{Q(t)} + \overline{K}.Q(t))$$

JK flip flop can be implemented using two 3-input Fredkin gate and a Pauli X-gate which is the quantum equivalent of CMOS NOT gate.

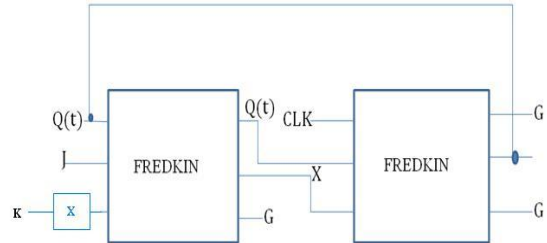


Fig 15: Proposed JK Flip Flop using Reversible Gates

T flip flop is implemented using a CNOT and a 3-input Fredkin gate. The derived equation of T flip flop is given by

$$Q(t + 1) = CLK.(T \oplus Q(t)) + \overline{CLK}.Q(t)$$

The corresponding circuit diagram is shown below.

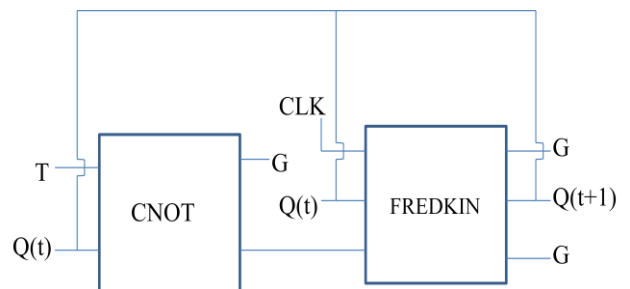


Fig 16: Proposed T Flip Flop using Reversible Gates

In the given quantum circuit, the CNOT is used for the operation $T \oplus Q(t)$ which is fed into the Fredkin Gate whose output is controlled by the CLK value.

5. RESULT ANALYSIS

The existing circuits [3][9][12][13] were compared with the proposed circuits. The comparison was done on the basis of the number of gates required to build the quantum circuits, and the quantum cost of the circuits and the number of Garbage outputs produced. The tables below show the comparison between the previous and proposed designs of D, JK and T flip flops based on the above mentioned parameters.

Table 1: Comparison of Different D Flip-flops

Parameters of Comparison	Previous Methods	Proposed Method
Number of Gates	6	3
Quantum Cost	3+	8
Number of Garbage Output	8	4

In [9], the proposed new gate i.e. the BME gate has a quantum cost of 5. The quantum cost of each circuit has been evaluated by summing the quantum cost of the individual gates required to build the circuit. Using the same approach, the quantum costs of JK and T flip flops have been calculated and the comparisons are shown below.

Table 2: Comparison of Different JK Flip Flops

Parameters of Comparison	Previous Methods		Proposed Method
Number of Gates	10	5	2
Quantum Cost	24+	15	11
Number of Garbage Output	12	4	3

Table 3: Comparison of Different T Flip Flops

Parameters of Comparison	Previous Methods		Proposed Method
Number of Gates	10	3	2
Quantum Cost	24+	11	6
Number of Garbage Output	12	3	2

The above tables validate that the proposed designs are optimized under all three aspects of comparison.

One aspect has to be kept in mind i.e. there is no provision for feedback in reversible logic. But, in order to implement flip-flops, a feedback path is required. Moreover, the delay in reversible circuits is almost negligible. So, the feedback path with considerable delay is forcefully introduced in the circuit. Otherwise, the circuit without the delay will not be able to detect the feedback path and hence will give an erroneous output. The functionality of all the circuits has been verified, considering the delay factor in the feedback path using Verilog and Modelsim.

6. CONCLUSION

The proposed reversible design is utilized for efficiently designing D, JK and T Flip-Flops. Flip-Flops are important memory elements and are used in several circuits like RAM, Logic Blocks of FPGA. By comparing the existing designs with the proposed ones, it has been observed that the proposed designs are less costly in terms of the number of gates and the number of garbage outputs. The proposed designs are highly optimized. Thus, the resulting reversible sequential circuits are more cost effective.

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