A Robust 10T SRAM Cell with Enhanced Read Operation

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ABSTRACT
This paper presents a new 10T SRAM cell that has enhanced read speed along with good read and write stability. While the read access time of the proposed cell is 0.72x and 0.83x smaller as compared to the two most popular 10T SRAM cells at 50^0C; the read SNM is 1.16x and 1.05x higher compared to existing 10T cells. Though the read-write power of the proposed cell is higher with respect to the existing 10T cells; nevertheless, it consumes lower power as compared to the conventional 6T cell. Layout using 45nm technology rule shows that the proposed cell consumes 15% smaller area as compared to popular Schmitt-trigger based 10T SRAM cell. Also, the results of Monte-Carlo simulation show that the proposed cell is more robust against process variations. Therefore, the proposed 10T SRAM cell can be used where the speed and robustness are the primary requirements.

General Terms
High speed SRAM cell, Robust SRAM cell, Differential Read-Write SRAM cell.

Keywords
6T-SRAM, 10T-SRAM, Access Time, Monte-Carlo Simulation, Noise Margin, Variability.

1. INTRODUCTION
Static random access memories (SRAMs) occupy a large portion of the total-die area and it is also predicted that nearly 94% of the total die area would be occupied by on-chip cache memory in near future nanoscale technologies [1]. Therefore, it is very important to increase the density of SRAM to enhance the overall system performance. Transistor sizing is used to maximise SRAM density and achieve a balance between conflicting requirements for stable read and write operations. However, increased variability in nano-CMOS technologies, especially intrinsic parameter fluctuations, can easily disturb this balance and may cause functional failure [2]. Consequently, it becomes extremely difficult to simultaneously balance the read-stability (read SNM) and the write-ability (write SNM) requirements of a 6-transistor (6T) cell. SRAM cell with ten transistors have been proposed to address this issue [3], [4]. The existing 10T SRAM cells use extra transistors to decouple the read and write path that allows tuning of read SNM and write SNM independently. While the existing 10T cells provide a high read SNM, they have the disadvantage of larger read access time. Therefore, this paper proposes a novel 10T SRAM cell that is faster and more robust than the existing 10T cells.

The rest of this paper is organized as follows. Section 2 presents the proposed SRAM cell operation along with basic review of standard 6T SRAM cell. In Section 3, simulation results are discussed and various performance metrics of our SRAM cell are compared with the existing 10T cells. Finally section 4 concludes this work.

2. SRAM CELLs
The operation and design of the conventional 6T and that of the proposed 10T SRAM cells are presented in this section. First the standard 6T SRAM cell is described and the associated challenges are highlighted, subsequently, the proposed 10T SRAM cell is introduced.

2.1 Conventional 6T SRAM Cell
A conventional 6T SRAM cell is shown in Fig. 1. Hold stability in the standby mode and read stability during a read operation are two main stability metrics of an SRAM. In a conventional 6T SRAM cell, the data storage nodes namely Q and QB are directly accessed through the access transistors (MAL & MAR) connected to the bit-lines. To maintain the data stability and functionality of a standard 6T SRAM cell, there must be constraints on the sizing of transistors. In order to maintain the read stability, the current produced by MNL and MNR must be higher as compared to the access transistors MAL and MAR. Alternatively, for write ability, the current conducting capability of MAL and MAR must be stronger as compared to MPL and MPR [5].

During a read operation in 6T SRAM, the storage nodes are disturbed due to the voltage division between the cross-coupled inverters and the access transistors; consequently, the stored data is disturbed. This is called 'read upset'. During this intrinsic disturbance produced by the direct data-read-access mechanism, the data is vulnerable to external noise (destructive read) [6]. A separate read bit-line and read path is used at the cost of increased cell area and increased read access time to address this issue [4]. Therefore the primary goal of this paper is to address the read stability issue in 6T SRAM circuits while maintaining lower read access time. The proposed 10T SRAM cell is described in the next section.

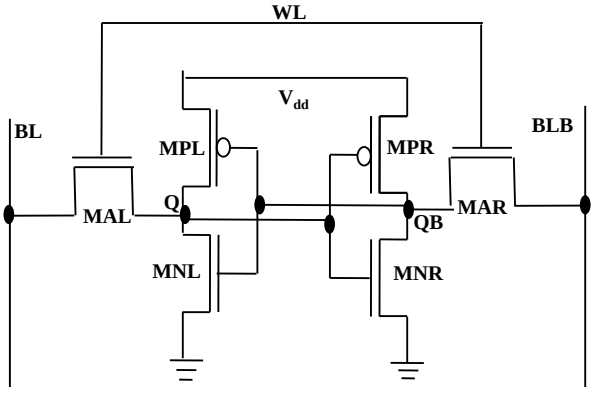

Fig. 1. 6T SRAM Cell

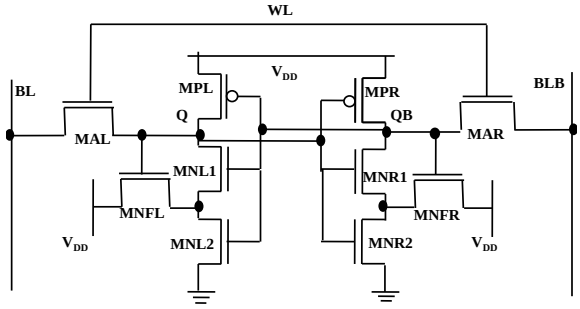

Fig. 2. Schmitt Trigger 10T SRAM Cell [3]

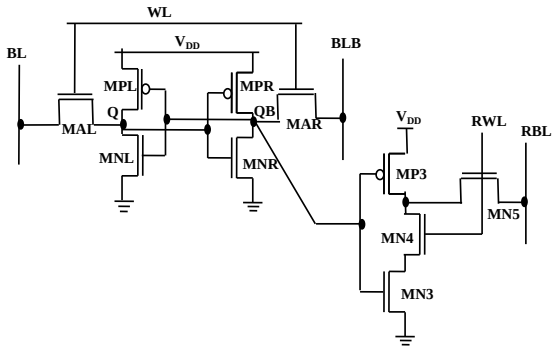

Fig. 3. 10T SRAM Cell [4]

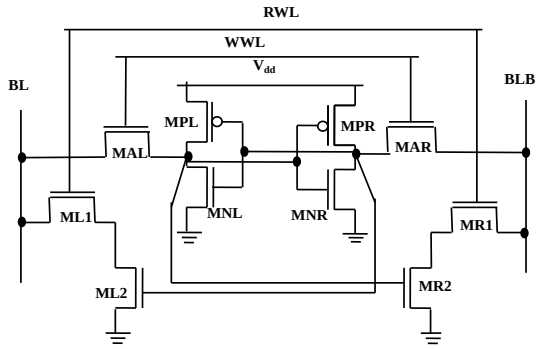

Fig. 4. Proposed 10T SRAM Cell

2.2 Proposed 10T SRAM cell

Single ended read SRAM [4] has longer read delay as compared to differential ended SRAM [3], as the later employs reading with sense amplifier. A 50 mV difference between the two bit-lines BL and BLB is good enough to be correctly detected by a sense amplifier [7]. In the conventional 6T SRAM cell, read and write operations take place through same access transistors, and hence both read and write failure cannot be avoided simultaneously due to conflicting requirements of transistor sizing. Fig. 4 shows the circuit diagram of the proposed differential-read 10T SRAM cell. The proposed circuit provides a differential read through different access path for read & write operations; therefore, it utilizes a differential sensing scheme for read operation. The proposed circuit saves cell area as it also utilizes the same bit-lines for both read and write operation contrary to the 10T cell in [4]. Moreover, by using separate path for read and write operations, allows independent tuning of read and write stability.

The proposed circuit utilizes the cross-coupled inverters (composed of MPL, MNL, MPR and MNR) similar to conventional 6T SRAM cell. The two write access transistors MAL and MAR are controlled by write word line (WWL). Whereas, the additional transistors ML2 and MR2 are controlled by the data stored in the cell and the two read access transistors ML1 and MR1 are controlled by a separate read signal (RWL). In the hold mode, WWL and RWL both are kept at ground that reduces the circuit to simple cross-coupled inverters. Thus, the hold SNM of the proposed SRAM cell is similar to that of the 6T cell.

During the write operation, the WWL is pulled to 'high' while the RWL is 'low'. Therefore, the write operation is similar to a conventional 6T cell. Since the proposed 10T SRAM cell has different read path, it can use wider access transistors to improve the writing ability in comparison with the conventional sizing method. It is also to be noted that the cell does not require any additional circuit for write; hence the write operation does not incur additional area and power penalties [8]. In the read mode, the RWL is pulled to 'high' while WWL is at 'low'. Therefore, MAL and MAR transistors are turned off and decouple the storage nodes from the write path. Assuming that node Q stores "1", then the MR2 will be ON and the BLB is discharged through MR1 and MR2. Alternatively, if QB stores "1", then the ML2 will be ON and the BL is discharged through ML1 and ML2. Since the read operation ideally does not involve the role of inverter transistor pair, the read SNM is enhanced almost to the level of hold SNM.

3. RESULT AND DISCUSSION

The proposed as well as all other cells analysed in this paper are sized such that the pull-up (PU) transistors are smaller than access (PG) transistors which in turn is smaller than the pull-down (PD) transistors. The transistor widths $W_{PU}/W_{PG}/W_{PD}$ are chosen as 32nm / 48nm / 64nm, respectively for the 6T cell. For a fair comparison, transistors of 6T portion (core) of all other 10T cells have the same dimensions as those of the 6T cell. Transistors ML1/MR1 and ML2/MR2 in the proposed cell have widths equal to 48 nm and 64 nm respectively. Transistors MNFL and MNFR in the Schmitt Trigger 10T (ST10T) SRAM cell, shown in Fig. 2, are sized at minimum width (i.e. 32 nm). All devices are of minimum length i.e. 32nm for this technology node. Thus, basic 6T portion of all the cells have *cell ratio* (CR) or β-ratio = 1.33 and *pull-up ratio* (PR) or γ-ratio = 0.67, where

$$CR = \frac{(W/L)_{MNL,MNR}}{(W/L)_{MAL,MAR}} \quad \text{and} \quad PR = \frac{(W/L)_{MAL,MAR}}{(W/L)_{MPL,MPR}}$$

Typically, CR of 1.2 – 3 is required to avoid read failure in a conventional 6T SRAM cell [5]. Similarly the write-ability of the SRAM cell is determined by the pull-up ratio (PR) or γ ratio. Generally, PR ≤ 1.8 is required to maintain good write-ability [5]. Therefore, to avoid read and write failure, CR = 1.33 and PR = 0.67 are maintained.

HSPICE [9] simulations with 32-nm Predictive Technology Model (PTM) [10] model are employed for comparing different SRAM cells. Monte-Carlo simulation is carried out to investigate the robustness of SRAM cells in the presence of process variations. The random variations contribute to threshold voltage fluctuation. Therefore, V_{th} is assumed to have independent Gaussian distributions with a 3σ variation of 10% [7]. As per ITRS, the expected variation in V_{DD} is 10% in future technology generations such as 22/16 nm [1]. Hence the different performance metrics are estimated by varying the supply voltage by ±10% around the nominal V_{DD} of 0.9 V. The variability (defined as the ratio of standard deviation (σ) to mean value (μ)) is a measure of robustness of an SRAM cell [11]. Lower the variability, more robust is the circuit. In the following sub-sections, various performance metrics of the proposed cell are compared with

conventional 6T, Schmitt trigger based 10T (hereafter called ST10T) [3], and Calhaun and Chandrakasan's 10T (hereafter called CK10T) [4].

3.1 Hold SNM

The SRAM cell's immunity to static noise is measured in terms of SNM. The SNM of a cell is defined as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit [6]. The hold SNM of SRAM cells is measured using the method described in [12]. Hold SNM determines the stability of the SRAM cell in standby mode. The basic structure of the cell (i.e. cross coupled inverters) in standby mode is similar in 6T, CK10T and the proposed 10T SRAM. The sizes of PU and PD transistors are also same. Therefore, the hold SNM for these three cells is found to be approximately same as shown in Fig. 5. On the other hand, ST10T uses feedback transistors to increase the inverter switching threshold whenever the node storing '1' is discharged to the '0' state. Thus, cell asymmetry changes and high hold SNM in ST10T is attributed to near-ideal inverter characteristic.

3.2 Read SNM

Read static noise margin (RSNM) is used to quantify the read-stability of the SRAM cells. It is SNM of the cell during read operation. In a conventional 6T SRAM, when node Q is at V_{DD}, QB does not remain strictly at ground but rises to some steady state voltage due to the voltage division between the access transistor and the pull-down transistor in the inverter. Therefore, there is a chance of read-upset. On the other hand, in the proposed 10T cell, if node Q is at V_{DD}, QB is maintained strictly at 0V due to the complete decoupling of the data storage nodes from the bit-lines during a read operation. Thus, by decoupling the data from the bit lines the cell stability is significantly enhanced in the proposed cell during the read operation.

As illustrated in Fig. 6, the read SNM of the proposed 10T SRAM cell is highest at all temperatures. It is to be noted that cells with RSNM of at least 25% of V_{DD} is generally considered to have excellent read stability [13]. The proposed cell shows a 10% higher RSNM than this minimum required value.

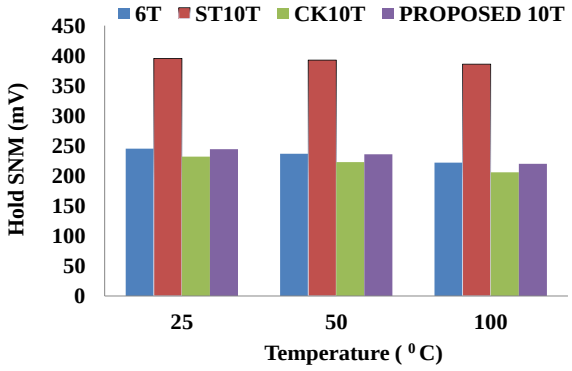

Fig. 5. Hold SNM at different Temperatures

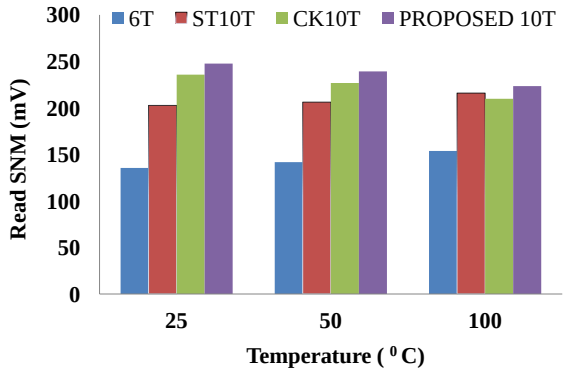

Fig. 6. Read SNM at different temperatures

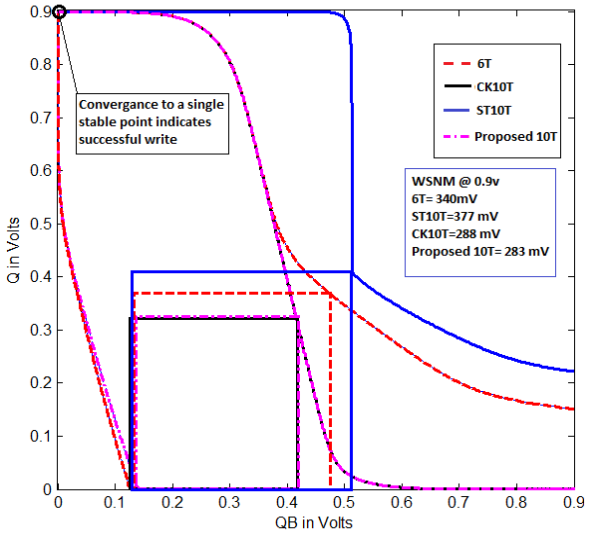

Fig.7. Static Voltage Transfer Characteristic to determine the Write SNM of an SRAM cell.

3.3 Write SNM

The write-ability of the SRAM cell can be determined in terms of Write SNM or WSNM. Write SNM is a measure of the ability of the cell to pull down a '1' storage node to a voltage less than switching threshold, V_M of the other inverter storing '0', so that flipping of the cell state occurs. The write SNM of a cell is graphically estimated using the read and write voltage transfer curve (VTC). The write VTC, while writing '0' to 'Q', is measured by sweeping Q (see Fig. 7, y-axis) with WL high and BL low and monitoring QB (see Fig. 7, x-axis). This write VTC is used in combination with the read VTC, which is measured by sweeping QB (see Fig. 7, x-axis) and monitoring Q (see Fig. 7, y-axis). The side length of the smallest square, which can be embedded between the read and write VTCs of the same SRAM cell at the lower half of the curves, passed the trip-pint of the left inverter, represents WSNM [14]. Fig.7 shows the voltage transfer characteristics of the SRAM cells to determine the write SNM.

When the write VTC intersects the read VTC at lower point, indicates a negative write SNM which signifies a write failure. As shown, 6T, ST10T, CK10T, and Proposed 10T show 340mV, 377mV, 288mV, and 283mV WSNM, respectively. The proposed bitcell shows 1.20 × (1.33×) fold smaller WSNM compared with 6T (ST10T). In CK10T and our proposed10T, there is no 'read upset' problem due to decoupled read path. Therefore the read VTC as shown in Fig.7 reaches to x-axis and a lower WSNM is observed.

However, very marginal difference (only 5mV) in WSNM is observed between CK10T and proposed 10T due to similar circuit during write operation. It is also to be noted that, the read and write VTCs converge to a single stable point, which signifies a successful write operation in the cell [7].

3.4 Read Access Time (TRA)

In case of differential-read SRAM cells, such as 6T cell, the read access time (T_{RA}) is the time required for discharging the bit-line (BL)/complementary bit-line (BLB) voltage to 50mV from its initial value after the wordline is turned on during a read operation. The 50-mV difference between BL and BLB is good enough to be detected by a sense amplifier, thereby, avoiding read-upset [15]. In case of single ended read (such as CK10T), the read access time is the time required for discharging the bitline voltage to half of Vdd after the word line is turned on during a read operation [16]. However, for fair comparison, we have used the read definition for the T_{RA} measurement of CK10T as suggested in [17] for single ended read operation. The actual T_{RA} for CK10T will be even more as it uses single ended read. The proposed bitcell shows read access time of 0.72x and 0.83x at 50^0C as compared to CK10T and ST10T cells respectively. This is because the existing 10T cells have three transistors (one PG + two PD in ST10T and two PG + one PD in CK10T) in discharging path, thereby, increasing read access time. Fig. 8 shows that the T_{RA} of the proposed cell is lower than ST10T and CK10T at all temperatures. The proposed cell has a delay penalty of only 16%; whereas, the ST10T and CK10T show 40% and 60% higher delay as compared to the delay of standard 6T SRAM cell.

3.5 Write Access Time (TWA)

Write Access time (T_{WA}) for writing '0' at node Q is the time required for node Q to fall to 10% of its initial voltage for '1' after the wordline is turned on during a write operation. Similarly, T_{WA} for writing '1' is the time required for node Q to rise to 90% of voltage value for '1' from its initial low level after the wordline is activated during a write operation. Since the core of the cell structure is similar in all the four SRAM cells during write operation, the write access time is almost same for all SRAM cells analysed in this paper. Nevertheless, as shown in Fig. 9, the proposed cell has 13% smaller write access time as compared to the ST10T SRAM cell at 50^0C.

3.6 Robustness Comparison

Continued miniaturization of CMOS technology has resulted into performance variability that is attributed to process variations [17]. Process variability has severely affected the performance of circuits designed at deep submicron technology nodes. Therefore, robustness of any circuit towards this variability has become an important figure-of-merit. The robustness of the proposed SRAM cell is compared with other cells using Monte-Carlo simulation. The variability of a performance metric of SRAM cells is defined as the ratio of the standard deviation (σ) to the mean value (μ) of that performance metric. Fig. 10 compares the variability in T_{RA}, T_{WA}, Hold SNM, and Read SNM in the presence of process variability. It is evident from Fig. 10 that the proposed SRAM cell is more robust to process variations as compared to other cells analyzed in this paper.

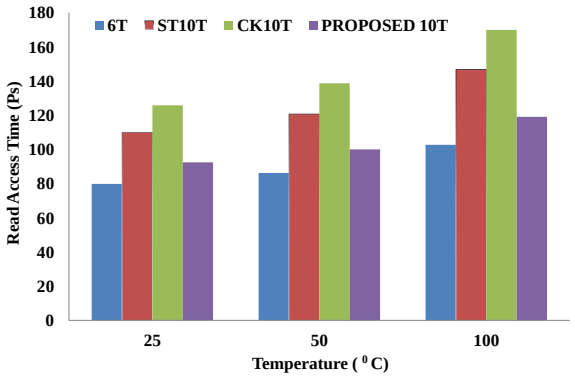

Fig. 8. Read Access Time at different temperatures

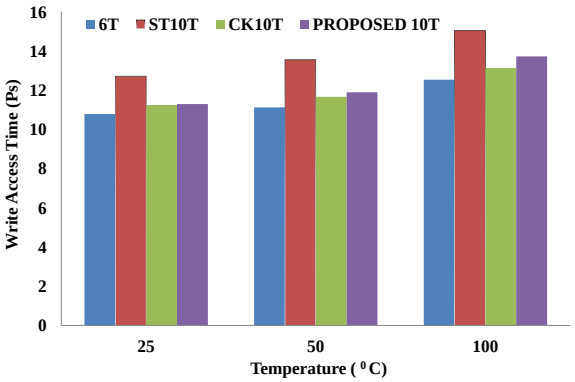

Fig. 9. Write Access Time at different temperatures

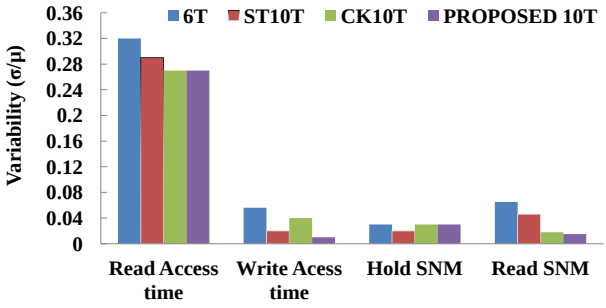

Fig. 10. Robustness comparison of SRAM cells

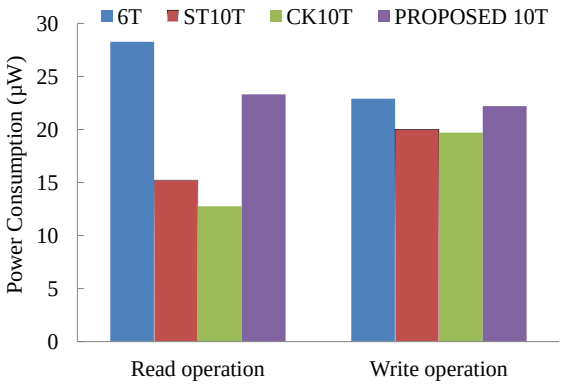

Fig. 11. Power Consumption for 'read' and 'write' operation

3.7 Read and Write Power Comparison

Fig. 11 depicts the power consumed by different SRAM cells while performing 'read' and 'write' operations. It is clear that the proposed SRAM cell consumes more power as compared to ST10T and CK10T cells. However, our cell

consumes 12% lower power as compared to the standard 6T SRAM cell. Moreover, the proposed cell consumes 2%, 4% and 7% more average energy per operation as compared to 6T, CK10T and ST10T SRAM cells respectively.

3.8 Area Comparison

Fig.12 shows the layout view of 6T, ST10T and the proposed 10T cell designed in a 45 nm technology rules. The cell areas are normalized to 6T SRAM cell. The proposed cell shows an area overhead of 55% compared with 6T SRAM cell. However proposed cell consumes 15% smaller area as compared to ST10T cell. The CK10T cell includes one extra PMOS which significantly increase the N-well area (layout not shown). Therefore the proposed cell does not include larger area overhead as compared to other 10T SRAM cells considered.

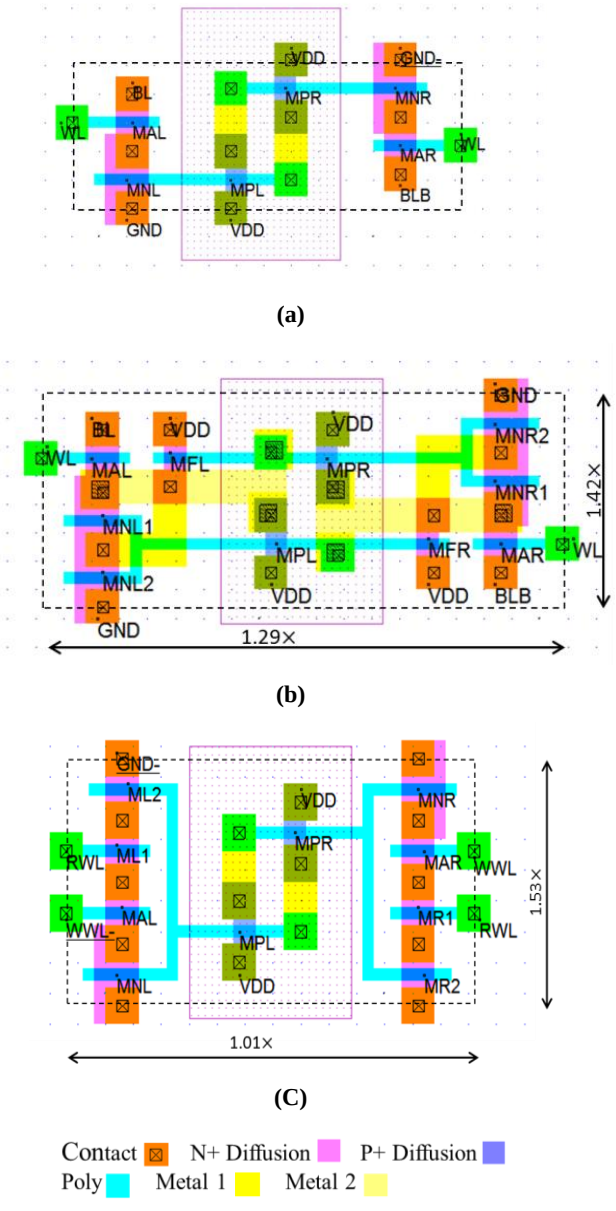

Fig.12. Layout of (a) 6T, (b) ST10T (c) Proposed 10T

4. CONCLUSION

In this work, a new 10T SRAM cell with differential read mechanism has been proposed. The proposed cell eliminates the conflicting design requirement of read versus write operation in a conventional 6T SRAM bitcell using separate read/write access transistors and the same bitlines. The proposed cell has 69%, 16% and 5% higher read SNM as compared to 6T, ST10T, and CK10T SRAM cells at 50°C. At the same time, our memory cell offers 17% and 28% higher read speed as compared to ST10T and CK10T cells. Monte Carlo simulations showed that the proposed cell offers a lower variability over standard 6T, ST10T, and CK10T SRAM cells, demonstrating its robustness. The proposed SRAM cell has a limitation of consuming slightly more energy per operation; nevertheless, it can be used in a scenario where speed and robustness are of prime concern.

5. REFERENCES

[1] International Technology Roadmap for Semiconductors (ITRS). [Online]. Available:http://public.itrs.net

[2] J. S. Rad, M. Guthaus, and R. Hughey, "Confronting the Variability Issues Affecting the Performance of Next-Generation SRAM Design to Optimize and Predict the Speed and Yield", IEEE Access, Vol. 2, pp. 577-601, 2014.

[3] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthresholdSRAM," IEEE Journal of Solid-State Circuits, vol. 42, no. 10, pp. 2303–2313, 2007.

[4] B. H. Calhoun, and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation", IEEE Journal of Solid-State Circuits, , Vol. 42, No. 3, pp. 680-688, 2007.

[5] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits:A Design Perspective*, 2nd ed. New Delhi, India: Prentice-Hall,2005.

[6] E. Grossar, M. Stucchi, K. Maex, W. Dehaene, "Read stability and write-ability analysis of SRAM cells for nanometer technologies" , IEEE Journal of Solid-State Circuits, vol. 41, no. 11, pp. 2577–2588, 2006.

[7] A. Islam and Mohd. Hasan, "Leakage Characterization of 10T SRAM Cell," IEEE Transactions on Electron Devices, vol. 59, no. 3, pp. 631–638, 2012.

[8] Roghayeh Saeidi, M. Sharifkhani and K.Hajsadeghi, "A Subthreshold Symmetric SRAM Cell With High Read Stability", IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 61, no. 1, pp. 26-30, 2014.

[9] Synopsys HSPICE User guide, Simulation & Analysis, 2012.

[10] Berkeley Predictive Technology Model, 2013. Website, 〈http://www.eas.asu.edu/~ptm〉 .

[11] A. Islam, and Mohd. Hasan, "A technique to mitigate impact of process, voltage and temperature variations on design metrics of SRAM Cell", Microelectronics Reliability, vol. 52, No. 2, pp. 405-411, 2012.

[12] E. Seevinck, F.J. List, J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells", IEEE Journal of Solid-State Circuits, vol. 22, no. 5, pp. 748–754, 1987.

[13] A. E. Carlson, "Device and circuit techniques for reducing variation in nanoscale SRAM," Ph.D. dissertation, University of California Berkeley,Berkeley, CA, May 2008.

[14] Z. Guo, A. Carlson, L.-T. Pang, K. T. Duong, T.-J. K. Liu, and B. Nikolic, "Large-scale SRAM variability characterization in 45 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 3174–3192, Nov. 2009.

[15] O. Okobiah, S. P. Mohanty, E. Kougianos, and M. Poolakkaparambil, "Towards robust nano-CMOS sense amplifier design: a dual-threshold versus dual-oxide perspective", . Proceedings of the 21st edition of the Great Lakes Symposium on VLSI, pp. 145-150, 2011.

[16] S. Lin, Y.-B. Kim, and F. Lombardi, "Design and analysis of a 32nm PVT tolerant CMOS SRAM cell for low leakage and high stability," Integr. VLSI Jornal, vol. 43, no. 2, pp. 176–187, Apr. 2010.

[17] G. Pasandi, S. M. Fakhraie, "A 256-kb 9T near-threshold SRAM with 1k cells per bitline and enhanced write and read operations", IEEE Transactions on VLSI Systems, vol. PP, no. 99, pp. 1-9, 2015.

[18] Samar K. Saha, "Compact MOSFET modeling for process-variability aware VLSI circuit design", IEEE Access, vol. 2, pp. 104-115, 2014.