Rational Sampling Rate Converter using Coefficient Symmetry

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ABSTRACT

In this paper, we proposes an efficient structure for rational sampling rate converter. Finite impulse response filter is used in between upsampler and downsampler in order to avoid image spectra and aliasing effects respectively. Coefficient symmetry of the linear phase filter is used so that number of required multiplication per output sample is reduced.

Keywords

FIR filter, linear phase, multirate system, rational sampling rate conversion.

1. INTRODUCTION

The need for digital products are growing day by day. Most of the industries like audio, video, and cellular rely heavily on digital technology. Digital signal processing plays main role in digital technology. Different sampling rates are used for different applications. The efficiency of the overall system is improved by using more than one sampling rate. Systems which employ more than one sampling rates are called multirate systems. When sampling rate is increased is called interpolation, and when decreased is called decimation. Decimator is denoted by M and interpolator is denoted by L. Sampling rate can be reduced by a factor of *M* is achieved by discarding every *M-1* samples and can be increased by a factor of *L* by inserting *L-1* zeros into the output stream. Combining interpolator and decimator with low pass filter results in rational sampling rate converter. The block diagram of rational sampling rate converter is as shown in Fig.1.
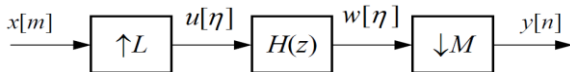

Fig. 1. Rational sampling-rate converter.

Fig. 1 shows that the input signal is upsampled by factor of L, after that signal is filtered by transfer function H(Z), and resulting signal is downsampled by a factor of M. A filter is used in between decimation and interpolation to suppress aliasing and to remove imaging respectively [16].

The relation between input sampling rate f_{in} and output sampling rate f_{out} is given by

$$f_{out} = \left(\frac{L}{M}\right) f_{in}$$

(1)

$$H(z) = \sum_{k=0}^{N} h_k z^{-k}$$

(2)

Where

$$h_{N-k} = h_k \qquad k = 0, 1, ..., N$$

(3)

H(z) is transfer function of linear phase FIR filter. Design of sampling rate converter [1] based on least square method.

Resampling realization method is used for better accuracy of signal resampling. Number of required multiplications can be reduced by using linear phase prototype filter building a nearly perfect reconstruction cosine modulated FB utilizing coefficient symmetry [2]. The alternatives for use of MCM in polyphase decomposed interpolation and decimation FIR filters is shown in [3]. It represents that by using the proposed matrix-vector multiplication, improvement is shown in terms of area, sample rate, and power consumption.

Another decimation filter without multipliers is proposed in [4] is based on FIR filter and rounding and sharpening techniques. The polyphase decomposition is applied to the rounded interpolator and its polyphase components are moved to the lower rate.

High throughput Sample Rate Converters (SRC) find applications Software Defined Radio (SDR) where a large degree of flexibility is required to support varied sample rates [5]. By designing frequency-response masking approach filters building the FB so that the periodic filters are evaluated at the input sampling rate and the masking filters at the output sampling rate. The design and implementation complexity can be reduced when compared with other existing techniques [6].

In paper [7] a hybrid approach is proposed for GSM digital down converter using multiplierless and multiplier based decimators. The proposed structure reduces the cost, filter order and hardware complexity.

The design and optimization of an ultra- high speed Digital Down Converter (DDC) is designed by FPGAs. The necessary optimizations to achieve an efficient implementation in state of the art FPGAs are explained and a case study for an FPGA optimized Digital Down Converter design suitable for OFDMA systems is presented [8].

In paper [9] GSM based digital down converter is proposed which uses optimal equiripple technique to reduce resource requirement and polyphase decomposition to improve hardware complexity and also reduces the pass band droop as well as increase the attenuation in folding band of CIC filter. A high speed interpolator using embedded LUT structure for software defined radios increases the speed and also save the resources.

Decimator design has been presented for multirate digital signal processing. It is observed from the simulated results that symmetric structure consumes almost 50% less multipliers and MPIS compared to transposed structure. So the symmetric structure based decimator in [10] is suitable to provide cost effective solution.

Multiplier-less technique is presented in [11] to implement a high speed CIC decimator. It is designed for wireless applications like SDR and GSM. The Cascaded Integrator Comb is a commonly used decimation filter which performs

sample rate conversion (SRC) using only additions/subtractions. The speed of proposed design is enhanced by utilizing embedded LUTs.

Another method is presented to design & implement GSM based digital down convertor for **S**oftware **D**efined **R**adios [12]. Optimal equiripple technique is used in proposed DDC to reduce the resource requirement. A polyphase decomposition structure is used to improve the hardware complexity of the system design. The proposed model is implemented by using embedded multipliers, LUTs and BRAMs of target device which enhance the performance of system in terms of speed and area.

An efficient method has been presented to implement high speed and area efficient interpolator for wireless communication systems [13]-[14]. A multiplier less technique is used which employ multiply-and-accumulate operations with look up table (LUT) accesses. In this paper [15] optimized decimator has been presented to improve the implementation complexity. The proposed decimator is implemented using Matlab as standard FIR, Half Band FIR and Nyquist FIR by using the multistage design techniques. The performance of different decimator designs is compared in terms of error and hardware requirements. Different implementations of FIR filter for sampling rate converters are presented in [16],[17]and [18].

This paper is organized as follows: Section 2 shows basic relations of sampling rate converter. Section 3 gives design simulations with an example. Section 4 shows generalization form of sampling rate converter. Implementation complexity is shown in section 5 and some concluding remarks are given in section 6.

2. RATIONAL SAMPLING RATE CONVERTER

2.1 Basic Input Output Relations Between Input And Output Samples

For the sampling rate converter shown in Fig 1, the time domain relations are given as

$$u[n] = \begin{cases} x\left[\dfrac{n}{L}\right] & for\ n = 0, L, 2L,... \\ \\ 0 & otherwise \end{cases} \tag{4}$$

$$w[n] = \sum_{k=0}^{N} h_k u[n-k] \tag{5}$$

$$y[n] = w[Mn] \tag{6}$$

Where hk's are coefficients of the transfer function H(z). The direct combination of (3a)-(3c) is following:

$$y[n] = \sum_{k=0}^{N} h_k x\left[\frac{Mn-k}{L}\right] \tag{7}$$

2.2 Input-output relations in Matrix Form

Based on (7), the (n+kL) th output sample, with k being an integer, is

$$y[n+KL] = \sum_{k=0}^{N} h_k x\left[\frac{M(n+KL)-k}{L}\right]$$
$$= \sum_{k=0}^{N} h_k x\left[\frac{Mn-k}{L} + KM\right] \tag{8}$$

$$y[n+l] = \sum_{K_l=0}^{K_l^{\max}} h_{lM+(K_l-[lM/L])L}x\left[\frac{Mn}{L} - K_l + \left[\frac{lM}{L}\right]\right] \tag{9}$$

$$y[n+l] = \begin{bmatrix} h_{lM-[lM/L]L} \\ h_{lM-[lM/L]L+L} \\ \vdots \\ h_{lM+[(N-lM)/L]L} \end{bmatrix}^{T} \begin{bmatrix} x[m+\left\lfloor\dfrac{lM}{L}\right\rfloor] \\ x[m+\left\lfloor\dfrac{lM}{L}\right\rfloor-1] \\ \vdots \\ x[m-\left\lfloor\dfrac{(N-lM)}{L}\right\rfloor] \end{bmatrix} \tag{10}$$

For the rational sampling rate converter shown in fig (1)with rational factor L/M and a filter order N, L consecutive output samples, y[n+l] can be expressed by rewriting this as

$$y_{n,L} = H_{l\times(p+q+1)}x_{m+p,m-q} \tag{11}$$

$$y_{n,L} = \begin{bmatrix} y[n] & y[n+1] & y[n+2] & ...... & y[n+L-1] \end{bmatrix}^{T} \tag{12}$$

3. DESIGN SIMULATIONS

This section illustrates, with the help of example, the proposed approach for implementing a sampling rate converter by a rational sampling factor L/*M* in such a manner that the filter coefficient symmetry is used.

3.1 Rational Sampling Factor 3/5:

This section gives a rational sampling rate converter by factor L/M, as shown in Figure 1, with *L* = 3 and *M* = 5. The relation between the output samples *y*[*n*] and the input samples *x*[*m*] is shown in Figure 4. As seen from the figure, for every five input samples, three new output samples are generated. Three consequent output samples can be expressed in a matrix form as

$$\begin{bmatrix} y[n] \\ y[n+1] \\ y[n+2] \end{bmatrix} = \begin{bmatrix} 000h_0h_3h_6h_9h_{12}h_{10}h_7h_4h_1 \\ 00h_2h_5h_8h_{11}h_{11}h_8h_5h_200 \\ h_1h_4h_7h_{10}h_{12}h_9h_6h_3h_0000 \end{bmatrix} x_{m+3,m-8} \tag{13}$$

After some modifications, the above system can be transformed into the following form:

$$
\begin{bmatrix} y[n] \\ y[n+1] \\ y[n+2] \end{bmatrix} = \begin{bmatrix} 000 \\ 000 \\ h_1 h_4 h_7 \end{bmatrix} x_{m+3,m+1} + \begin{bmatrix} h_7 h_4 h_1 \\ 000 \\ 000 \end{bmatrix} x_{m-6,m-8} +
$$

$$
\begin{bmatrix} 0 \\ h_2 \\ 0 \end{bmatrix} (x[m+1] + x[m-6]) +
$$

$$
\begin{bmatrix} 101 \\ 010 \\ 10-1 \end{bmatrix} \begin{bmatrix} c_0 c_1 c_2 \, 000 \\ h_5 h_8 h_{11} \, 000 \\ 000 \, d_2 d_1 d_0 \end{bmatrix} x_{m,m-5}^{(2)}
$$

$$(14)$$

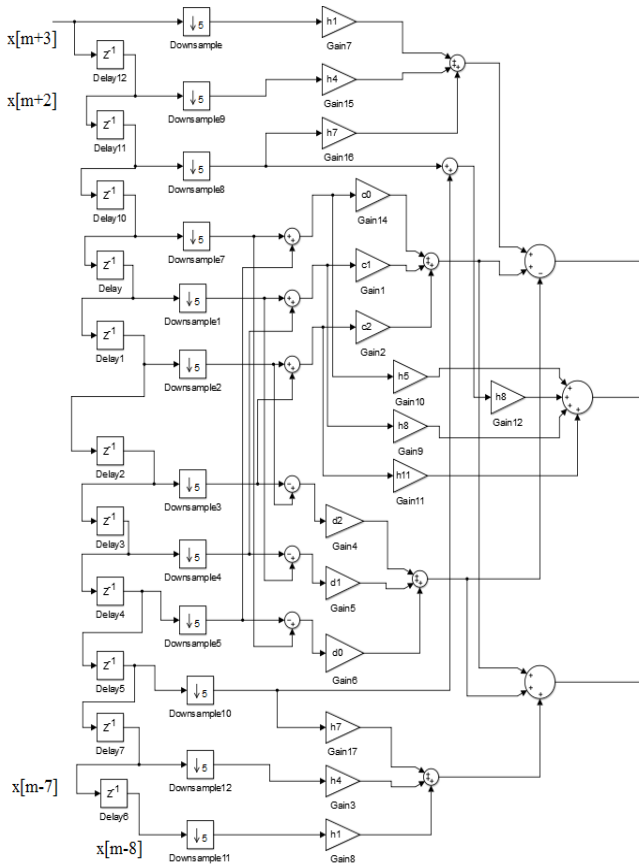For implementing (above), a structure can be derived.

Figure 2. Implementation structure for a rational sampling-rate converter by a factor of 3/5

Three output samples can be generated by utilizing coefficient symmetry are 12 multiplications and 22 additions. This means, for one output sample, 4 multiplications and 7.33 additions are required. And the implementation that does not utilize the coefficient symmetry requires 8.67 multiplications and 7.67 additions per output sample.

4. SAMPLING RATE CONVERTERS WITH RATIONAL CONVERSION FACTORS-GENERALIZATION

As seen from the examples in Section II, a slightly different implementation structures are achieved depending on the rational factors as well as the filter order. The main purpose of this section is to give guidelines on how to derive an efficient implementation structure.

Filter Orders

In order to provide a better approach for a given rational factor L/*M*, the filter orders are consider to have the following values

$$
N = M(L-1) + 2kL \tag{15}
$$

$$
N = M(L-1) + (2k+1)L \tag{16}
$$

For a given rational factor *L/M* and a filter order satisfying either (15) or (16), the input-output function for a rational sampling converter given in Figure 1 can be expressed as follows:

$$
\begin{bmatrix} y[n] \\ y[n+1] \\ \vdots \\ y[n+L-1] \end{bmatrix} = H_{L \times (p+q+1)} x_{m+p,m-q} \tag{17a}
$$

In order to generate an efficient implementation, the matrix, as given by (17b), and input-output relations, given by (17a), can be divided into two parts as

$$
\begin{bmatrix} y[n] \\ y[n+1] \\ \vdots \\ y[n+L-1] \end{bmatrix} = \begin{bmatrix} H_a H_c \end{bmatrix} \begin{bmatrix} x_{m+p,m+1} \\ x_{m+p-q,m-q} \end{bmatrix} + H_b x_{m,m-q+p} \tag{18}
$$

After applying coefficient symmetry, the matrix $[H_a H_c]$ of size *L* by 2*p* becomes

$$
\begin{bmatrix} H_a H_c \end{bmatrix} = \begin{bmatrix} h_{-pL} \cdots & h_{-L} & h_{(L-1)M-L} \cdots h_{qL} \\ h_{M-pL} \cdots h_{M-L} & h_{(L-2)M-L} \cdots h_{M+qL} \\ \cdots \cdots & \cdots \\ h_{M+qL} \cdots h_{(L-3)M-L} & h_{M-L} \cdots h_{M-pL} \\ h_{qL} \cdots h_{(L-1)M-L} & h_{-L} \cdots h_{-pL} \end{bmatrix} \tag{19}
$$

It should be noted that most elements in the matrix $[H_a H_c]$ arezero-valued. Therefore, this matrix can be further optimized when used for implementing the overall system.By taking into account the coefficient symmetry, the matrix H_b of size *L* by q+1−*p* can be written as

$$H_b = \begin{bmatrix} h_0 & h_L & \cdots & h_{(L-1)M-L} & h_{(L-1)M} \\ h_M & h_{M+L} & \cdots h_{(L-2)M-L} & h_{(L-2)M} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ h_{(L-2)M} & h_{(L-2)M-L} & \cdots h_{M+L} & h_M \\ h_{(L-1)M} & h_{(L-1)M-L} & \cdots h_L & h_0 \end{bmatrix} \quad (20)$$

For $q+1-p$ being even, the above matrix is a centrosymmetric matrix [4], [5] and, therefore, it can be decomposed into one of the following two forms:

$$H_b = \begin{bmatrix} I_{\lfloor L/2 \rfloor} & 0 & J_{\lfloor L/2 \rfloor} \\ 0 & 1 & 0 \\ J_{\lfloor L/2 \rfloor} & 0 & -I_{\lfloor L/2 \rfloor} \end{bmatrix} H_{b_1} \begin{bmatrix} I_s & J_s \\ J_s & -I_s \end{bmatrix} (21)$$

$$H_b = \begin{bmatrix} I_{\lfloor L/2 \rfloor} & J_{\lfloor L/2 \rfloor} \\ J_{\lfloor L/2 \rfloor} & -I_{\lfloor L/2 \rfloor} \end{bmatrix} H_{b_2} \begin{bmatrix} I_s & J_s \\ J_s & -I_s \end{bmatrix} (22)$$

Where

$$S = (q+1-p)/2 \quad (23)$$

$$H_{b_1} = \begin{bmatrix} c_{1,1} & c_{1,2} & \cdots & c_{1,s} & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & & \cdots & \cdots & & \cdots & \\ c_{\lfloor L/2 \rfloor,1} & c_{\lfloor L/2 \rfloor,2} & \cdots c_{\lfloor L/2 \rfloor,s} & 0 \cdots 0 & 0 \\ h_{\lfloor L/2 \rfloor M} & h_{\lfloor L/2 \rfloor M+L} & \cdots h_{\lfloor L/2 \rfloor M+L(s-1)} & 0 \cdots 0 & 0 \\ 0 & 0 & \cdots 0 & d_{\lfloor L/2 \rfloor,s} & \cdots d_{\lfloor L/2 \rfloor,2} & d_{\lfloor L/2 \rfloor,1} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & 0 & d_{1,s} & \cdots & d_{1,2} & d_{1,1} \end{bmatrix}$$
$$(24)$$

$$H_{b_2} = \begin{bmatrix} c_{1,1} & c_{1,2} & \cdots & c_{1,s} & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & & \cdots & \cdots & & \cdots & \\ c_{L/2,1} & c_{L/2,2} & \cdots c_{L/2,s} & 0 \cdots 0 & 0 \\ 0 & 0 & \cdots 0 & d_{L/2,s} \cdots d_{L/2,2} & d_{L/2,1} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & 0 & d_{1,s} & \cdots & d_{1,2} & d_{1,1} \end{bmatrix}$$

$$(25)$$

$$c_{k,l} = (h_{(k-1)M+(l-1)L} + h_{(L-k)M+(l-1)L})/2 \quad (26)$$

$$d_{k,l} = (h_{(k-1)M+(l-1)L} - h_{(L-k)M+(l-1)L})/2 \quad (27)$$

$$x_{m,m-q+p}^{(s-1)} = \begin{bmatrix} I_s & J_s \\ J_s & -I_s \end{bmatrix} \begin{bmatrix} x_{m,m-s+1} \\ x_{m-q+p-s+1,m-q+p} \end{bmatrix} \quad (28)$$
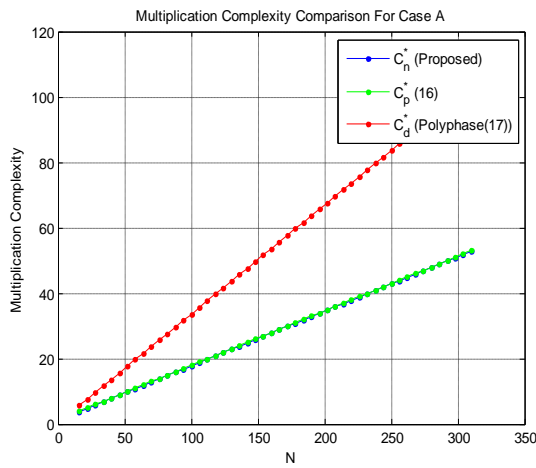
5. IMPLEMENTATION COMPLEXITY

Proposed technique shows that the implementation complexity of system is smaller than the system where the coefficient symmetry is not utilized.

The proposed implementation complexity approaches the desired goal as shown in TABLE I. For order $N = 23$, the number of multiplications required by the proposed implementation is only 60.4% of that required by the direct implementation that does not exploit the coefficient symmetry, whereas for $N = 212$, this figure reduces to 51.2%.

$$H_{L*(p+q+1)} = [H_a H_b H_c] = \begin{bmatrix} h_{-pL} & \cdots & h_{-L} & h_0 & h_L & \cdots & h_{(q-1)L} & h_{qL} \\ h_{M-pL} & \cdots & h_{M-L} & h_M & h_{M+L} & \cdots & h_{M+(q-1)L} & h_{M+qL} \\ h_{2M-pL} & \cdots & h_{2M-L} & h_{2M} & h_{2M+L} & \cdots & h_{2M+(q-1)L} & h_{2M+qL} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ h_{(L-1)M-pL} & \cdots & h_{(L-1)M-L} & h_{(L-1)M} & h_{(L-1)M+L} & \cdots & h_{(L-1)M+(q-1)L} & h_{(L-1)M+qL} \end{bmatrix}_{(17b)}$$

TABLE 1: Implementation complexity for rational sampling rate converter by 3/5 in number of multiplications(C*) and additions(C+)per output sample

|	Proposed		Paper[16]		Polyphase[17]		Comparison			
N	Cn*	Cn+	Cp*	Cp+	Cd*	Cd+	Cn*/Cp*	Cn+/Cp+	Cn*/Cd*	Cn+/Cd+
211	36.33	59.00	37.00	61.33	70.66	69.66	0.982	0.962	0.514	0.847
214	36.83	59.83	37.33	62.33	71.66	70.66	0.987	0.960	0.514	0.847
23	4.83	6.5	4.33	8.00	8.00	7.00	1.115	0.813	0.604	0.929
209	35.83	58.16	35.33	70.00	70.00	69.00	1.014	0.831	0.512	0.843
210	36.33	59.00	36.00	71.66	70.33	69.33	1.009	0.823	0.517	0.851
212	36.33	59.00	36.00	71.33	71.00	70.00	1.009	0.827	0.512	0.843
213	36.33	59.83	36.33	72.33	71.33	70.33	1.014	0.827	0.516	0.851

(a)
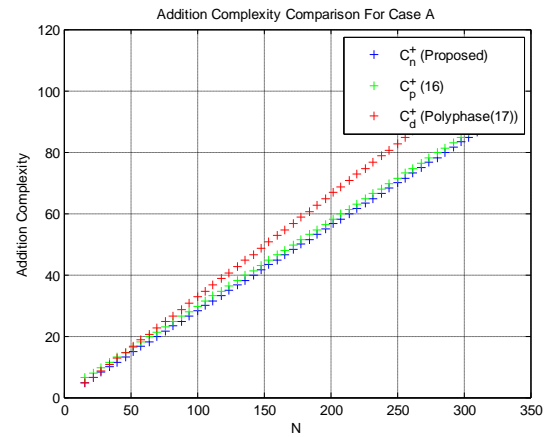
(b)
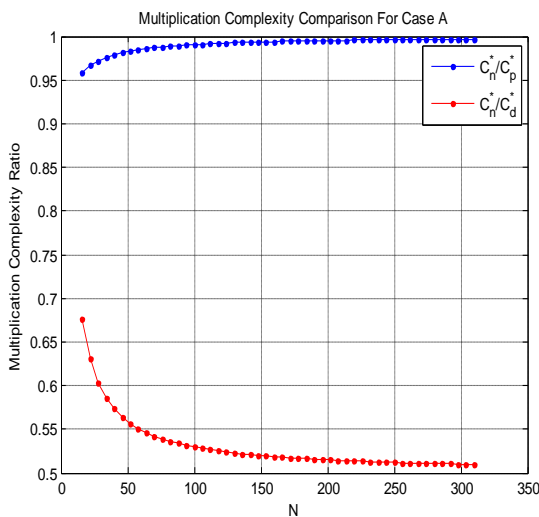
(c)
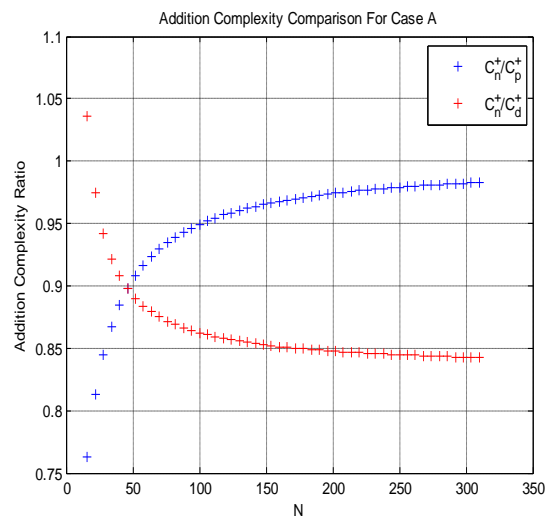
(d)

Fig. 3 Implementation complexity for rational sampling rate converters by 3/5 for case A(i.e. N=M(L-1)+(2k+1)L) (a) Number of multiplications(C*) per output sample. (b) Number of additions(C+) per output sample (c) Comparison between for multiplication (d) Comparison for addition complexity
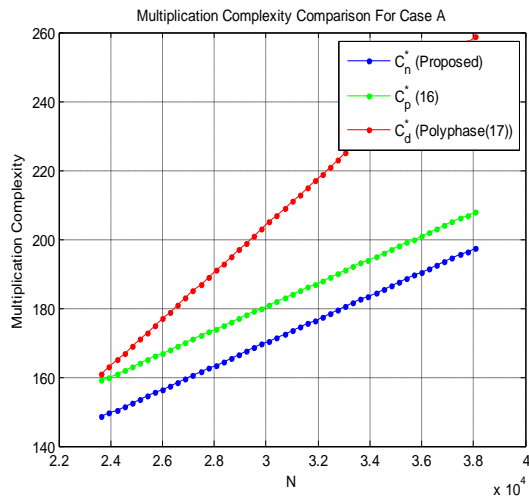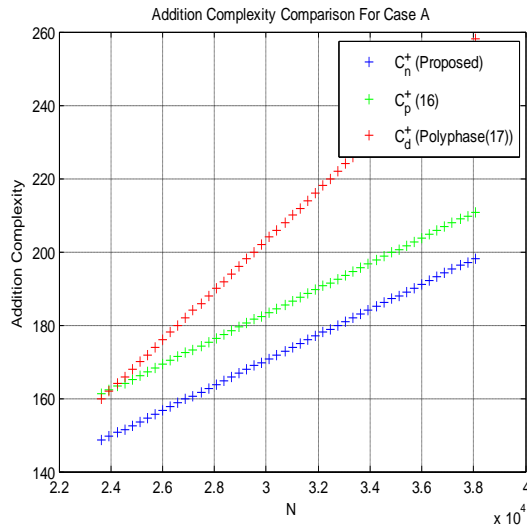
(a)   **(b)**

Fig. 4 Implementation complexity for sampling rate converter by 147/160.(a) Number of multiplications per output sample. (b) Number of additions per output sample.

6. CONCLUDING REMARKS

In this paper an area efficient and cost efficient sampling rate converter has been designed and simulated with the help of MatLab. The proposed method shows less number of multiplications as compare to polyphase [17] and [16] implementation. Finally the implementation complexity of proposed approach is evaluated and with the help of some examples, efficiency of the proposed implementation is compared with others. However for future implementation the proposed method can be applied to multistage rational sampling rate converter. Secondly, proposed method can be implemented in hardware also.

7. REFERENCES

[1] Yu Huijun, "Design Of A Sample-Rate Converter Based On Least-Square Method", IEEE International Conference on computer science and Information processing, pp. 332-335, June 2012.

[2] Robert Bregovic, Ya Jun Yu and Ari Viholainen, "Implementation of Linear-Phase FIR Nearly Perfect Reconstruction Cosine-Modulated Filter banks Utilizing the Coefficient Symmetry", IEEE Transactions on circuits and systems, Vol. 57, No. 1, pp. 139-151, January 2010.

[3] Oscar Gutafsson and Hakan Johanson, " Implementation of polyphase decomposed FIR filters for interpolation and decimation using multiple constant multiplication techniques", IEEE Asia Pasific conference on circuits and systems, pp. 924-927, 2006.

[4] Jeffrey P. Long and Jose A. Torres, " High Throughput Farrow Re-samplers Utlizing Reduced Complexity FIR Filters", IEEE International Conference on military communication, pp. 1-6, 2012.

[5] Gordana Jovanovic Dolecek, and Naina Rao Nagrale, "On Multiplier less fir decimation filter design," IEEE Conference on Electronics, Circuits and Systems, pp. 967-970, 2007.

[6] Bregovic, R.; Yong Ching Lim; Saramaki, T., "Frequency Response Masking Based Design of Two-Channel FIR Filterbanks with Rational Sampling Factors

and Reduced Implementation Complexity", IEEE International Conference on Image and Signal Processing and Analysis, pp. 121-126, 2005.

[7] G. Molina Salgado, and G. Jovanovic Dolecek, "Nonrecursive comb decimation filter with an improved alias

[8] rejection," IEEE Latin America Symposium on Circuits andSystems, pp.1-4, 2012.Robert Bregovic, Tapio Saramaki, Ya Jun Yu, and Yong Ching Lim, "An Efficient Implementation of Linear-Phase FIR Filters for a Rational Sampling Rate Conversion", IEEE International Conference on circuits and systems, pp. 453- 498, 2006.

[9] Rajesh Mehra, Swapna Devi, "FPGA Based Design of High Performance Decimator using DALUT Algorithm", ACEEE International Journal on Signal and Image Processing, Volume 1, pp. 9-13, 2010.

[10] Rajesh Mehra, and Lajwanti Singh, "cost analysis and simulation of decimator for multirate applications," International Journal of Computers & Technology, vol. 11, no. 1, pp.2175-2181, 2013

[11] Rajesh Mehra and Rashmi Arora, "FPGA-Based Design of High Speed CIC Decimator for Wireless Applications", International Journal of Advanced Computer Science and Applications, Vol. 2, No.5,pp. ,2011.

[12] Rajesh Mehra and Swapna Devi, "Efficient Hardware Co-Simulation of Down Converter for Wireless Communication Sysrems", International Journal of VLSI Design and communication Systems, Volume 1, No. 2, pp. ,June 2010.

[13] Rajesh Mehra and Ravinder kaur, "Reconfigurable Area and Speed Efficient Interpolator using DALUT Algorithm", Advanced in Networks and Communications, Volume 132, pp.117-125, 2011.

[14] Rajesh Mehra , "FPGA Design of Optimized CIC Interpolator for DSP Based Wireless Communication System", IMS MANTHAN Journal of Mgt., Computer

Science and Journalism, Volume 5, Issue-2, pp. 43-46, 2010.

[15] Rajesh Mehra and Swapna Devi "Optimized Design of Decimator for Alias Removal in Multirate DSP applications", Nonlinear System and Wavelet Analysis, pp. 100-103, 2010

[16] Robert Bregovic, Ya JunYu, Tapio Saramaki, " Implementation of Linear-Phase FIR Filters for a Rational Sampling-Rate Conversion Utilizing the Coefficient Symmetry", IEEE Transactions on circuits and systems, Vol. 58, No. 3, pp. 548-561, MARCH 2011.

[17] C-C Hasiao, "Polyphase filter matrix for rational sampling rate conversion", IEEE International Conference on Speech, Signal Process, pp. 2173-2176, April 1987.

[18] Yong Ching Lim. "An Efficient Implementation of Linear-Phase FIR Filters for a Rational Sampling Rate Conversion", IEEE International Symposium onCircuits and Systems ISCAS-06, 2006.