Review of SOI MOSFET Design and Fabrication Parameters and its Electrical Characteristics

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ABSTRACT
In current scenario the device count in an IC is running into billions per chip, the issue of power dissipation in the chip is becoming too critical. Due to decreasing device dimension the performance of the bulk Si MOSFET is limited by its fundamental physical limitation like reduction in carrier mobility due to impurities, p-n junction leakage current increases as the junction become more and more shallow and increasing gate tunneling effect as the gate oxide thickness decreases. These requirements have led to development of alternating technology. SOI (silicon on insulator) technology is an alternative choice of Conventional Technology which offers the performance as may be expected from the next generation technology. SOI technology offers significant advantages in fabrication, design and performance for many semiconductor circuits such as excellent isolation, radiation hardness, improved latch up free operation, reduced short channel effects, improved switching speeds and reduced leakage current, due to reduction in the drain-body capacitance. The reduction in the parasitic capacitances provides improved switching speed and superior performance. This paper is focused on the brief of SOI MOSFET Technology, its characteristics, advantages and disadvantages of it.

Keywords
SOI, MOSFET, CMOS, wafer, Silicon, Insulator

1. INTRODUCTION
During 1960s the need for radiation hardness devices in the devices in the defence and space industries lead the innovation of SOI devices. Due to lackness of proper fabrication process use of expensive material made it unpopular in the primary stage. However it has the characteristic to be an alternating technology due to the drawback of traditional bulk technology; its use in the prior stage become impractical due to technological deficiency and its expensive fabrication cost. The performance of bulk Si MOSFET is limited by the fundamental physical limits such as reduction in carrier mobility due to impurity, as the gate oxide thickness decreases the gate tunneling effect increases and the junction become more and shallower by increasing p-n junction leakage current. According to the Moore law which states that the performance of the processors are doubled every 18 month. Increasing the number of device count means decreasing the space of the device dimension which leads increasing the switching speed of the device. The important criteria used for measuring the performance of a circuit are speed and area. Although due to increased transistor density and the need of portable devices the most important cost measure in VLSI design is power consumption. SOI technology utilizes the low power technique. Most of the early SOI MOSFET was fabricated with SOS (Silicon On Sapphire) wafers technology. The unique feature of today's SOI wafer is that they have a BOX or buried silicon oxide layer across the entire wafer. Introducing a BOX structure in conventional MOS structure provides a lot of improved characteristic such as excellent isolation, reduced leakage current, reduced short channel effects, improved latch up free operation, improved switching speed due to reduction in the drain body capacitance and radiation hardness. SOI CMOS technology is likely to be an alternative for deep sub-micron CMOS [2]. It appears to be the best option for low-power electronics.

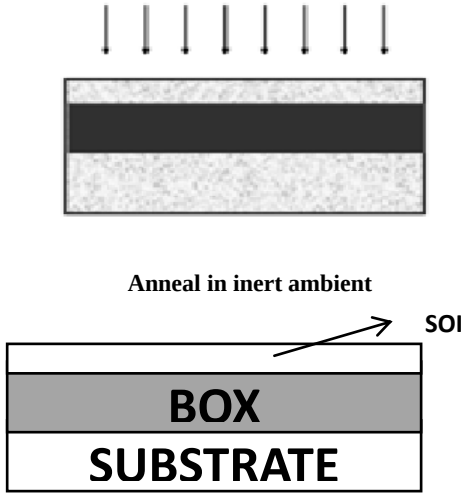
2. HISTORICAL PERSPECTIVE OF SOI MOSFET
SOI technologies can be in categorized in two groups. In the first, a thin insulating layer is used to separate the active semiconductor layer from the semiconductor substrate. These include zone melting recrystallization (ZMR), Separation by implantation of oxygen (SIMOX), full isolation by porous oxidized silicon (FIPOS), and wafer bonding (WB).

In other group, the semiconductor material film is deposited directly onto an insulating substrate. This happens in Silicon On Sapphire (SOS) and Silicon on zirconia (SOZ).

2.1 Separation by implantation of oxygen (SIMOX) :
In 1966, Watanabe and Tooi [1] observed in laboratory that if oxygen ions are implanted into silicon using a RF gas discharge then the resulting silicon dioxide has the characteristics identical to thermally grown SiO2. In 1978, it was discovered that if energy and dose of oxygen is kept 150 KeV and 12 x 1018 cm2 and the sample is annealed at a temperature of 1150ºC, then the resulting buried oxide layer exhibits excellent electrical characteristics and the top Si layer is crystalline. This method is known as SIMOX process, illustrated in figure 2.1.

The silicon layer above the BOX is where the device is fabricated, and the silicon below the BOX, called the handle, is un-doped silicon that is only used for handling the wafer during the fabrication process, and does not affect device performance. The BOX, greatly affects the parameters of device, and lead to the development of new structure types.

(Oxygen implanted at: energy 120-200KeV DOSE~ 0.3-1.8e18 Cm2)



Above 1300ºC, 3-6 hours

- BOX thickness: 100, 200, 400 nm
- SOI film thickness varies from 50-240 nm

Fig: 2.1 SIMOX process

The BOX gave rise to some new structure types not available through the bulk silicon technology. One of the more unusual is the double-gate device, or volume inversion MOSFETs (VI-MOSFET). These devices have a second gate located in the buried oxide layer, which may be grounded. By using second voltage this gate can be turned on and off. Another arrangement is stacked devices, which makes SOI devices in a 3-Dimensional structure. This can be used for parallel processing, and lead to faster processing times. The BOX helps insulate the devices from one another so they do not interfere with each other. A third type of device is the Nano-SOI device which is too thin, which have a silicon thickness of less than 10nm [4]. This is possible due to the noise-reducing capabilities of the BOX. During 1980s, the recrystallization of Si layer with laser or e-beam was studied extensively and also formed a part of Japanese R & D project aimed at developing 3D ICs. This project also included fabrication and evaluation of SOI substrates, design and simulation of SOI devices, and circuit design technology for 3Dimensional ICs [2].

In the same tenure, there was an important improvement in SIMOX technology. It was discovered that if the annealing temperature is raised to above 1300ºC , then the dislocation density is reduced from 109 cm-2 to 106 cm2 [3]. During 90s, SIMOX process was further improved with the discovery of "dose window"[4] which resulted in drastic reduction in dislocation density and buried oxide thickness was increased by high temperature oxidation (ITOX technology) [2]. The resulting SIMOX technology led the throughput to increase by a factor of 5 and dislocation density as low as 102 cm2 to 103 cm2.

2.2 Zone Melting Recrystallization (ZMR):

ZMR [5] technology produces SOI structures by recrystallization of polysilicon films, deposited on oxidized silicon wafers. In the ZMR process, a thermal oxide (1-2 µm thick) is first grown on a bulk silicon substrate, followed by polycrystalline silicon film (0.5-1.0 µm thick) on the thermal oxide. The whole structure is capped with a 2 µm thick layer of deposited thermal oxide covered by a thin Si3N4 layer. A melting zone is scanned across the entire silicon wafer. As a result, full liquid phase recrystallization of silicon wafer can be carried out in a single pass.

2.3 Full Isolation by Porous Oxidation Of Silicon (FIPOS):

FIPOS [6] involves the use of oxidized porous silicon. This technique is more complicated than the SIMOX and ZMR, but offers the potential for essentially defect-free active silicon layers. This process is relatively clean. Oxidation of the porous silicon layer leads to the standard thermal oxide and does not disturb the high quality of the original silicon film. The key aspect in FIPOS technique is the formation of porous silicon, which is controlled by the type and concentration of doping as well as by the current density and HF solution.

2.4 Wafer Bonding (WB)

The WB [7] technique provides undamaged crystal quality and more flexibility than SIMOX for both the Si film and the buried oxide layer. There are three basic steps required for the WB process: (1) mating two silicon wafers at room temperature, (2) annealing the bonded wafers at temperatures above 800ºC for several hours to increase bonding strength, and (3) thinning down the wafers to a proper thickness by grinding and polishing and/or etching.

One prominent example of a wafer bonding process is the Smart Cut method which was developed at CEA-LETI, one of the world's premier microelectronics research laboratories. Smart Cut is a revolutionary technique used to transfer ultra-thin single crystal layers of wafer substrate material such as silicon onto another surface. Differing from traditional layer-transfer techniques uses a thermal activation process. It slices the wafer horizontally from the donor substrate through lifting off a thin layer and placing it onto a new substrate. Inherently, this process offers better control, and a single donor substrate might be reused several times for further layer transfers. The transferred layer thickness is pre-determined by the cleavage zone created through ion implantation (of hydrogen, helium, argon, etc.). After the layer transfer and bonding the cleaved surface of the thin film is treated, and annealed to ensure a silicon film (in the case of SOI) and surface quality near to silicon prime wafers. Smart Cut is Soitec's patented process technology for creating engineered wafers. Engineered wafers (like Silicon-On-Insulator or SOI) consist of multiple layers of substrate materials.

The main drawback of the wafer bonding technique is its difficulty in producing very thin, uniform Si film through the traditional polishing technique. Hence the third step is becoming more and more important for manufacturing ultrathin Si films with good uniformity.

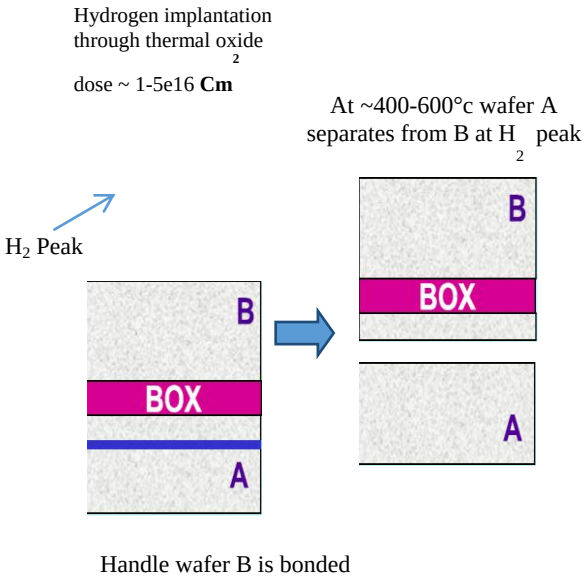


Fig: 2.2 smart cut processes

2.5 Silicon On Zirconia (SOZ) & Silicon On Sapphire (SOS):

The sapphire (alpha-Al203) crystals [8] are produced using either the flame-fusion growth technique, edge-defined film-fed growth or Czochralski growth. The first two of these techniques provide sapphire boules which have to be sliced before polishing and the third technique provides thin rectangular sapphire ribbons, which have to be cut into circular wafers later on. After chemical and mechanical polishing, the sapphire wafers receive a final hydrogen etching at 1150ºC in an epitaxial reactor and a silicon film is deposited using pyrolysis of silane at a temperature between 900 and 1000ºC.

Due to thermal mismatch and lattice, defect in density in films is quite high, especially in very thin films. The main drawbacks present in the as grown SOS films are aluminum auto doping from the Al2o substrate and stacking faults. These results the low values of resistivity, mobility, and lifetime near the interface.

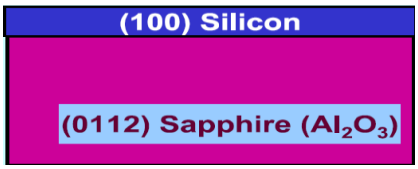


Fig: 2.3 silicon on sapphire

As the scaling of device dimension requires thinner and thinner top Si layer, various research methodologies were made to develop SOI wafers with top Si layer with small but highly uniform thickness (thickness variation < 10%). It results a plasma assisted chemical etching (PACE) process [9] and ELTRAN process [10] were developed in 1992 and 1994 respectively.

The structure of an SOI MOSFET, as shown in figure 1.5 is similar to the conventional bulk MOSFET with the exception that the active silicon layer is separately insulated from the bulk silicon substrate by a thick buried oxide layer.

Depending on the silicon film thickness and the channel doping concentration, two types of SOI MOSFETs can be distinguished

Thick film Silicon on Insulator (SOI) and

Thin film Silicon on Insulator (SOI)

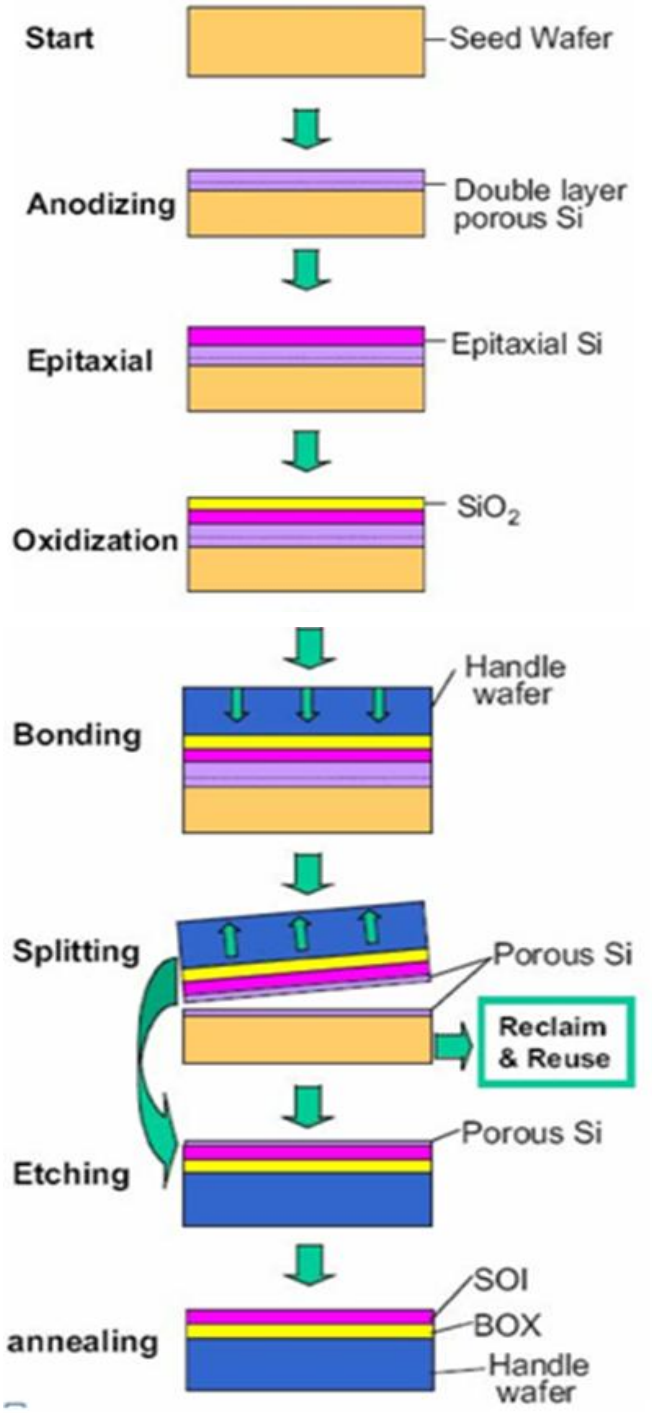


Fig: 2.4 ELTRAN Process

3. OPERATION OF SOI MOSFET

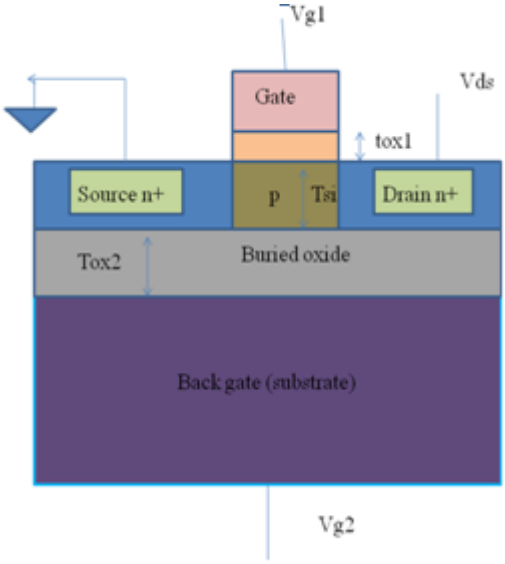


Fig: 3.1 Structure of an SOI n-MOSFET

In a thick-film SOI device the silicon material thickness is larger than twice the max. depletion width, Xdmax

$$x_{d\max} = \sqrt{\frac{4\varepsilon_{Si}\Phi_F}{qN_A}}$$

Where, Φ F is the fermi potential as given below:

$$\Phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

As a result, there is no interaction between the depletion regions arising from the back and front interfaces and a neutral body of silicon material exists beneath the front depletion zone.

If we connect it to the ground through a body contact the device operations will same as of a conventional device. If the body is left electrically floating, it will behave as a conventional device, except the floating body effects.

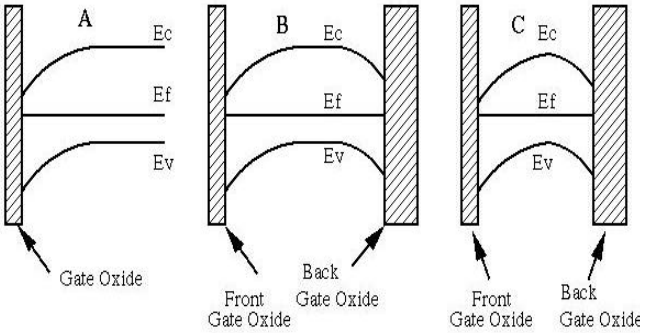


Fig: 3.2 Band Diagram in a bulk (A), a thick-film SOI (B), and a thin-film SOI Device (C)

In a thin-film Silicon on Insulator device the silicon film thickness is smaller than X d max. The film is fully depleted at threshold, with respect of the back-gate bias (with the exception of a possible presence of thin accumulation or inversion layers at back interface). Among every type of SOI MOSFETs, fully depleted SOI devices having back interface depleted which exhibit the most important properties such as excellent short channel behavior, a quasi-ideal sub-threshold slope, low electric fields and high trans-conductance.

Medium thickness SOI device is an intermediate case between thin and thick film device, and is obtained when X d max < t si < 2 X d max, t si being the film thickness. If the back gate bias results the front and back depletion zones to coalesce, the device behaves like a thin film device otherwise it will behave as a thick-film device.

In PD MOSFET, a part of the body region remains undepleted or neutral on the other hand in FD MOSFET, whole of the body, the depletion region extends right up-to the body and BOX interface. Hence in Fully Depleted SOI MOSFET the complete body region is depleted off majority carriers.

3.1 Threshold Voltage

For a thick-film SOI device, which behaves like a bulk device due to absence of interaction between the front and back depletion regions, the threshold voltage remain same as in a bulk device and is given as:

$$V_{th} = V_{FB} + 2\Phi_F + \frac{qN_a x_{d\max}}{C_{ox}}$$

Where, VFB is the flatband voltage,

ΦF is the fermi potential, and

x dmax is the maximum depletion width.

For a thin-film SOI device, the expressions for threshold voltage like a function of the different possible steady-state charge conditions at the back interface are given as [18]

$$V_{th1,inv2} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + 2\Phi_F - \frac{Q_{depl}}{2C_{ox1}}$$

$$V_{th1,depl2} = V_{th1,acc2} - \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si}+C_{ox2})}(V_{G2} - V_{G2,acc})$$

$$V_{th1,acc2} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + (1+\frac{C_{Si}}{C_{ox1}})2\Phi_F - \frac{Q_{depl}}{2C_{ox1}}$$

Where,

Q s2 is the charge in possible back inversion or accumulation layer,

ϕs1 and ϕ s2 being the potentials of front and back silicon/oxide interfaces,

ϕs1 and ϕs2 being front and back work functions respectively.

3.2 Output Characteristics

The expression of the current characteristics ID (VG1 , VG2 , VDS) of a thick-film SOI MOS transistor is identical to a bulk MOSFET with some modifications due to the parasitic bipolar effects coming up due to the presence of an floating body. The derivation of the current characteristics of a thin film, fully

depleted SOI device can be done [18] using assumptions of the classical gradual channel approximation [11]. The saturation current in an SOI MOSFET is given as:

$$I_{Dsat} \cong \frac{1}{2}\frac{W}{L}\frac{\mu_n C_{ox1}}{(1+\alpha)}(V_{G1} - V_{th})^2$$

Where:

$$\alpha = \frac{C_{Si}}{C_{ox1}}$$

(for fully depleted device in accumulation)

$$\alpha = \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})}$$

(for fully depleted device in depletion)

$$\alpha = \frac{\varepsilon_{Si}}{x_{d\max} C_{ox}}$$

(for partially depleted and bulk devices)

Since, α fully depleted SOI < α bulk < α back accum SOI, the drain saturation current is highest in the fully depleted device than bulk device, and the device with back accumulation. The high saturation current in a thin-film, fully depleted SOI MOSFETs brings about an increase in current drive, which contributes to enhanced speed of fully depleted SOI CMOS circuits.

4. SOI CHARECTERISTICS

In a bulk MOS transistor, only the top region of the silicon wafer is relevant for electron transport. SOI structures emerged from the idea of isolating the active device overlay from the influence of the underlying silicon substrate by a buried oxide layer.

4.1 Dielectric Isolation

SOI circuits consist of single device, dielectrically isolated from each other and from the substrate. Each device sits alone on the top of the insulator, there are no leakage paths to the substrate or to the adjacent devices. This allows both analog and digital devices to be used on the same chip. The inter-device distance is much more shrinkable in SOI than in bulk.

This critical limitation of bulk technology for VLSI circuits is due to unavoidable proximity of diffused regions that belong to adjacent components. Sophisticated techniques of trench isolation are necessary to avoid latch-up in bulk silicon technology. Latch-up refers to unintentional activation of parasitic devices.

In figure 4.1 the superposition of PNP and NPN transistors, which have the common diffused regions, is a thyristor which causes uncontrollable high currents and leads to circuit failure when turn on. while, SOI is naturally free from latch up problem.

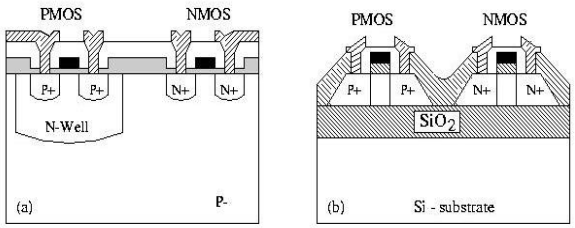


Fig: 4.1 Schematic configurations of CMOS transistors in bulk and SOI wafers

4.2 Vertical Junctions

In regular SOI films, the source and drain regions extend to the insulator, and only their lateral sides serve as junctions the surface of junction is much smaller than in bulk silicon. The smaller surface brings a substantial reduction in parasitic capacitances, and in propagation delays and dynamic power consumption. In short, for predefined power consumption, faster and much denser circuits can be integrated on SOI wafers.

4.3 Short Channel Effects

In small geometry MOS transistors, the source and drain junction induced depletion zone become relatively significant and impede the gate control through the whole space charge region they impede the gate control. A number of small channel effects like threshold voltage roll-off, punch-through drain induced barrier lowering originate due to the "charge sharing" between gate and junctions and degradation of sub-threshold slope. SOI devices are more immune to short-channel effects [12]. Basically, the extension of source/drain depletion regions is restricted by the junction size and the dual gate control of the surface potential.

4.4 Reliability

The primary motivation for developing SOI technologies was their excellent tolerance of transient radiation effects. The incoming particles generate electron-hole pairs in proportion to the volume of device. These photocurrents act as leakage currents, causing charge collection and soft errors. It dramatically reduced in SOI as the volume exposed to carrier generation is 2-3 orders of magnitude smaller than in bulk Si, due to the presence of buried oxide layer in these devices. When ionizing radiation flows through a transistor, it creates a tail of mobile charge particles on its wake which increases with the path length of the radiation. Since mobile charges can't be created there hence the buried insulator layer lessens the amount of mobile charge that is generated.

4.5 High integration density and simplified process

Silicon on Insulator CMOS offers a higher integration density than bulk CMOS. This high density results mainly from the absence of wells in Silicon On Insulator technology. SOI CMOS devices can be isolated by oxidation, on the other hand bulk devices normally use junction isolation.

4.6 Reduced parasitic capacitances

SOI CMOS devices are isolated from each other dielectrically. Such isolation reduces the parasitic junction capacitance. In a bulk CMOS device the parasitic junction capacitance consists of two components: the channel stop implant under the field oxide and the capacitance between the drain and the substrate. There is only one cornponent of parasitic capacitance between junction and the substrate in SOI device. As the thick BOX layer (greater than 300nm) is

taken in SOI, capacitance is much smaller than its corresponding counterpart in a bulk device. The reduction of parasitic junction capacitance contributes to the excellent speed performance observed in SOI CMOS circuits.

The presence of the buried oxide not only reduces the junction capacitance, it reduces other parasitic capacitances as well (it means al1 the parasitic capacitances between the silicon substrate and the various terminals [13].

4.7 Sub-threshold performance

Inverse sub-threshold dope can be related by equation:

$$S = \frac{\partial V_G}{\partial log I_{Ls}} = 2.3\frac{kT}{q}\left(1 + \frac{C_{depletion}}{C_{ox}}\right)$$

It is a function of the ratio of $C_{depletion}$ to C ox in a bulk Si CMOS technology, while scaling down the channel length results in a roll-off of the threshold voltage, which is called short channel effect. This causes due to the loss of control by the gate to part of the depletion zone below it. To rninimize the short channel effect, one should increase the doping level in channel region. It increases Cd and hence an increase in Inverse sub-threshold slope. In a PD SOI structure, short channel effects are not so serious as in bulk Si CMOS. Therefore optimization of channel doping profile to achieve better inverse sub-threshold dope with minimum channel effects. In a thin film SOI device, the channel region is fully depleted. It results as an inverse sub-threshold slope in FD SOI MOSFET. For low-power low-voltage applications the lower inverse sub-threshold slope is highly desirable because it allows the use of devices with a smaller value of threshold voltage without an increase in leakage current. This reduces the static power consurnption significantly.

5. CHALANGES IN SOI TECHNOLOGY

It is generally acknowledged that SOI CMOS provides better device performance than its bulk counterpart. However, the presence of the BOX layer also results in self-heating, floating body effects etc.

5.1 Self-Heating Effects

Due to thermal isolation of substrate through the buried insulator in an SOI transistor, removal of excess heat generated by the Joule effect through the device is less efficient than in bulk which leads to substantial elevation of device temperature [14]. The excess heat mainly diffuses vertically through the buried oxide and laterally through the silicon into the contacts and metallization. The device heats up to 50 to 150ºC due to the relatively low thermal conductivity of the buried oxide. This increase in device temperature leads to a reduction in mobility and current drive, thus degrading the device performance over a period of time [15][16].

5.2 Floating Body and Parasitic Bipolar Effects

The existence of a floating volume of silicon beneath the gate is at the origin of several effects related to SOI, generally referred to as floating body effects [17]. There exists a parasitic bipolar transistor in the MOS structure. If we consider an n-channel device, the N+ source, the P-type body and the N+ drain form the emitter the base and the collector of an NPN bipolar transistor, respectively. The base of the bipolar transistor is normally grounded by means of a substrate contact in a bulk device. But, due to the floating body in an SOI MOSFET base of the bipolar transistors is electrically floating region. Thus parasitic bipolar transistor is origin of several undesirable effects in SOI devices.

5.3 Kink Effect

When Vds increases, electron-hole pairs are generated due to impact ionization. Electrons can easily move into the drain region while holes migrate to the floating body, at the place where the potential is low. Because of the existence of the buried oxide layer Holes cannot be extracted through the substrate and are trapped in the neutral region. The accumulation of holes increases the potential in the bulk and decreases in the threshold voltage. Resulting a kink is observed in saturation region.

The injection of holes into the floating body forward biases the source-body diode. Floating body reach a positive potential, as given by the following equation [18]:

$$I_{holes,gen} = I_{s0}\left(exp\left(\frac{qV_{BS}}{nkT}\right) - 1\right)$$

Where:

I holes, gen is the hole current generated near the drain,

I so is the saturation current of the source-body diode,

VBS is the potential of the floating body,

n- is the ideality factor of the diode.

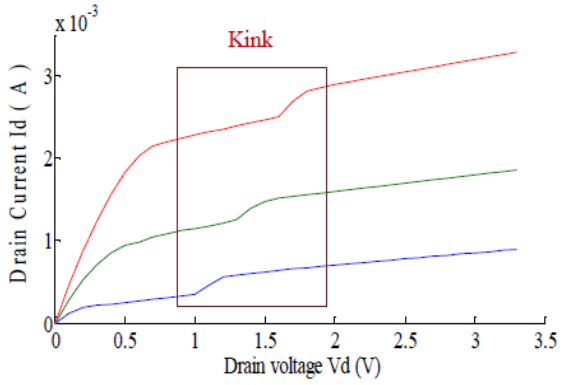


Fig: 5.1 Kink effect in SOI MOSFET structure

5.4 Single transistor latch-up

Due to the floating body existence, lateral bipolar action become more frequent in SOI MOSFET. Due to impact ionization near channel-drain junction the base current in the parasitic bipolar is formed. In NMOSFET the parasitic BJT effects are more serious than that in PMOSFET; the reason behind this is the impact ionization which is more pronounced in NMOSFET rather than PMOSFET.

In bulk NMOSFET, the holes generated by impact ionization flow as substrate current. By the way holes generated by impact ionization are trapped in the neutral region in the SOI structure. When the rninority carrier lifetime in the silicon film is high enough, the parasitic NPN BJT presented in the NMOSFET device can amplify the base current(i.e. the hole current generated by impact ionization near the drain). It results in an increase of drain current. As a result, when the current is higher than certain level, the parasitic BJT will be dominant.. The gate may even lose the control to source drain current. The phenomenon is referred as the single transistor latchup [19]. Generally it may cause malfunction of the circuit. Notice that such effect only happens when VDS is

larger than VGS – Vth, since the impact ionization only occurs when the device operates in saturation region.

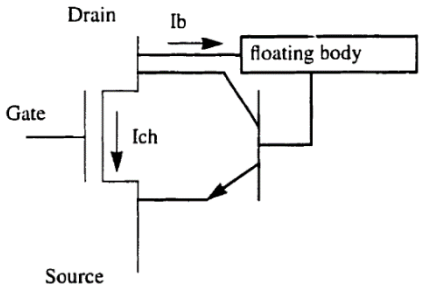


Fig: 5.2 Parasitic NPN bipolar junction transistors in SOI NMOSFET structure.

5.4 Reduced drain breakdown voltage

Because of the existence of parasitic BJT structure in SOI NMOSFET the current generated by the impact ionization is amplified. This results in the reduced breakdown voltage of SOI NMOSFET. Normally larger the beta value of parasitic BJT, the smaller the breakdown voltage. Such reduction of breakdown voltage is more significant in short channel devices and when the good lifetime SOI materials are used, since the beta in such kind of devices is much larger than unity [20].

6. CONCLUSION

As the silicon on insulator technology becomes mainstream technology it becomes more important to compensate and handle for the challenging issues like kink effect, self -heating effect, short channel effect etc. using SOI. Although various methods has been already presented to reduce the kink effect like SELBOX structure but it need to be more precise for the better frequency response.

In comparison with traditional bulk technology SOI technology need to be more suited for the nanometer and low supply voltage technology. It is also expected that the power consumption should decrease.

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