Full adder Design using Hybrid Technology

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ABSTRACT
Full Adder is a fundamental element that is used in all the processor for not only in ALU but in various part of the chipset. The work proposes a Hybrid design methodology to contribute the requirements for the designing of full adder with reduced delay. The Analysis of the designed full adder is done at 27^0C and 70^0C temperature range in CMOS 120 nm, 90 nm, and 50 nm technologies using Microwind tool. The result shows the comparison between different CMOS technologies in terms of delay and power dissipation. A comparison is also done in terms of delay of the designed adder with previously known adder cells, which shows the advantage of the proposed design.

Keywords
Full Adder, Hybrid design, Transmission gate (TG), CMOS technologies, pass transistor logic (PTL), power delay product (PDP), arithmetic and logic unit (ALU).

1. INTRODUCTION
Adder is a very basic building block of any kind of processor starting from arithmetic and logic unit to the other parts such as calculation of address, table indices, increment/ decrement and similar operations. Most of the VLSI applications, such as Digital Signal Processing (DSP), image processing, video processing and microprocessors extensively use arithmetic operations[1]. Binary addition is considered as the most important and crucial part of the arithmetic unit because all other arithmetic operations involve addition. So the full adder circuit need to be implemented in a very efficient manner considering the delay, power and area. And this will at last reduce the overall delay of the system. Here our man aspect is to design a full adder with low power high performance full adder[2][3].

The man goal of the work presented here is to design a full adder using a technique that is combination of pass transistor and transmission gate [4][5].

2. CIRCUIT TECHNIQUE
The fundamental circuit diagram of a full adder is shown below in Fig 1:

The logical expression to represent the 1-bit full adder is

$$SUM = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + BC_{in} + AC_{in}$$

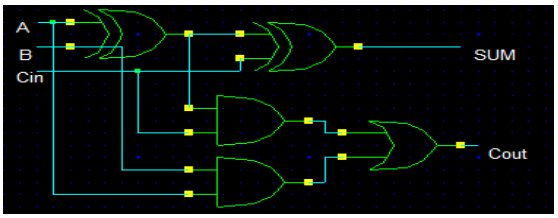

Fig. 1 Full adder of circuit diagram

3. PASS TRANSISTOR
Normally the basic function of transistor is a switch. But if the same transistor switch is configured so as to pass the logic level between the nodes then that is known as pass transistor logic. This actually reduced the number of transistor count by eliminating the unnecessary transistor. Because of this it reduced the number of active device needed. But at the same time it has the disadvantage that the voltage difference between the high and low logic level decreases at each stage which makes the cascading of pass transistor logic to use some logic to restore the signal voltage. Implementation of XOR gate require more transistor when implemented using simple gate logic, but if it has been implemented using PT require fewer gate[4][6].

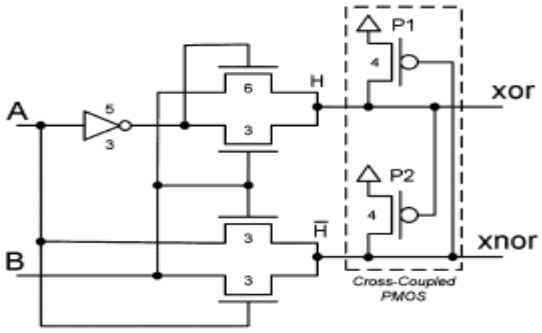

Fig. 2 XOR gate implementation using PTL

4. TRANSMISSION GATE
It is nothing but an electronic block that behaves similar to relay which can block or pass the signal based on the control signal provided to gate. It consists of two transistor NMOS and PMOS connected in parallel, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal. XOR based implementation using transmission gate full adder [7] is shown in fig. 3.

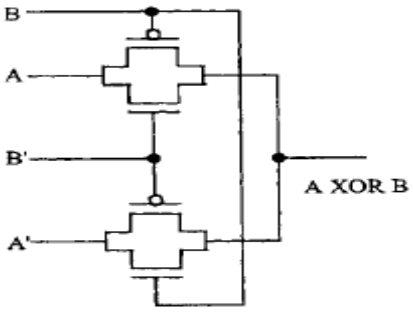

Fig. 3 XOR gate implementation using TG

5. PROPOSED PT AND TG BASED FULL ADDER

Pass transistor logic designing is an attractive approach as little number of transistors is required to implement various important logic functions. It is faster than conventional CMOS and also having an additional advantage of smaller transistor sizes and capacitances. A new sum circuit using pass transistor logic is proposed here. The design requires 8 Transistors to perform the sum function. While carry function is implemented using Transmission gate which also requires 8 transistors.

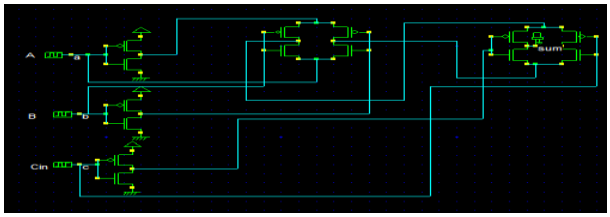

Fig. 4 Proposed SUM functional circuit

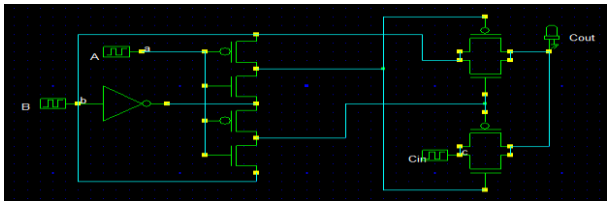

Fig. 5 Proposed CARRY functional circuit

A total of 16 Transistors are needed to implement the design. The advantage of having a Hybrid Design methodology helps in reducing the delay and area which overall reduce the overall PDP of the circuit.

6. LAYOUT DESIGN

Fig. 6 shows the layout of full adder using CMOS, Transmission gates and Pass transistors respectively

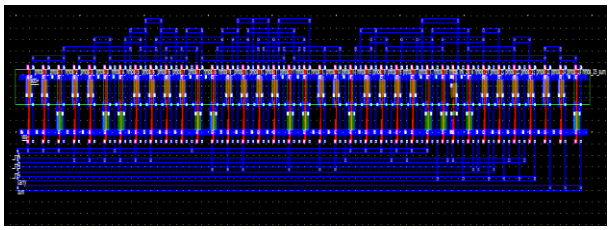

Fig 6 Layout of proposed Full Added Circuit in CMOS 120nm technology

7. SIMULATIONAND RESULT

Simulation of the proposed design has been performed in CMOS 120 nm technology in Microwind at room temperature ($27^{o}C$). Transistor sizes are kept at default for 120nm. The waveform of sum and carry is shown in fig. 7.

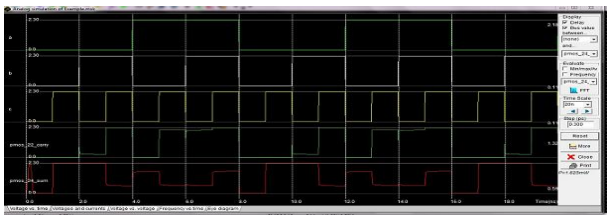

Fig. 7 Simulation result of Full adder in CMOS 120nm technology

Table 1 Analysis of Sum

SUM						
PARAMETRS	120 nm		90 nm		50 nm	
	27^0C	50^0C	27^0C	50^0C	27^0C	50^0C
VDD	2.3 V		2.3 V		1.4 V	
I/O	3.2 V		3.2 V		3.2 V	
P – WIDTH	0.72 µm		0.6 µm		0.68 µm	
P – LENGTH	0.12 µm		0.1 µm		0.08 µm	
N-WIDTH	0.24 µm		0.2 µm		0.24 µm	
N-LENGTH	0.12 µm		0.1 µm		0.08 µm	
POWER DESSIPATED	79.348 uW	82.726u W	126u W	214u W	17.690u W	21.721u W
A	10ps	11ps	11ps	12ps	7ps	7ps
B	10ps	11ps	11ps	12ps	7ps	7ps
C	10ps	11ps	11ps	12ps	7ps	7ps
WORST DELAY	10ps	11ps	11p	12ps	7ps	7ps

Table 2 Analysis of Carry

CARRY						
PARAMETRS	120 nm		90 nm		50nm	
	27	50	27	50	27	50
VDD	2.3 V		2.3 V		1.4 V	
I/O	3.2 V		3.2 V		3.2 V	
P - WIDTH	0.72 µm		0.6 µm		0.68 µm	
P -LENGTH	0.12 µm		0.1 µm		0.08 µm	
N-WIDTH	0.24 µm		0.2 µm		0.24 µm	
N-LENGTH	0.12 µm		0.1 µm		0.08 µm	
POWER DESSIPATED	10.736 uW	11.250 uW	15.270 uW	28.100 uW	1.995 uW	2.542 uW
A	7ps	7ps	4ps	4ps	4ps	4ps
B	7ps	7ps	4ps	4ps	4ps	4ps
C	7ps	7ps	4ps	4ps	4ps	4ps
WORST DELAY	7ps	7ps	4ps	4ps	4ps	4ps

The simulation is performed in Microwind tool for different CMOS technologies 120 nm, 90 nm, 70 nm and 50 nm. Varying Voltage ranges for VDD and input output is given in Table 4 for Sum and Table 5 for Carry for all technologies, which allowed us to compare the speed degradation that is the delay of newly designed adder topology. The results of the

designed Full Adder circuits in this work are compared with a reported previous standard CMOS full adder circuit as shown in Table 6. The temperature of operation for circuits is kept at 27^0C to 70^0C. Default values of the channel width (W) and length (L) for NMOS and PMOS for all technology are taken as shown in Table 1 and 2. By the proposed design it is possible to reduce the delay of the adder without significantly increasing the power consumption, and default transistor sizes for all technologies can be set to achieve minimum power delay product (PDP).

On comparing the results obtained in Table 3 in terms of area and propagation delay with previous work [4] a reduction in area and delay is obtained in the proposed adder. The proposed adder have least number of transistor count as compared to other adders designed previously in [4][8].

Table 3 Comparison in Terms of Delay with Previous Work

Design	Delay in ps	
	Temp 27^0C	Temp 70^0C
C-CMOS [4]	539 ps	542 ps
Hybrid [4]	762 ps	862 ps
14T [4]	54 ps	57 ps
10T [4]	47.6 ps	48.2 ps
SERF [4]	47 ps	49 ps
XOR 4T based [4]	42 ps	46 ps
Proposed adder worst case delay at V_{dd}1.20V for 120nm	24 ps	26 ps
Proposed adder worst case delay at V_{dd}1.20V for 90nm	34 ps	34 ps
Proposed adder worst case delay at V_{dd}2.5V for 120nm	23 ps	25 ps
Proposed adder worst case delay at V_{dd}2.5V for 90nm	17 ps	21 ps
Proposed adder worst case delay at V_{dd}1.2V for 50nm	31 ps	30ps

8. CONCLUSION

The newly designed full adder is an example of Hybrid-CMOS design style. Pass transistor with CMOS logic is presented in this work that targets reduced Delay and Power delay product with adder. A performance analysis in terms of Delay is presented for 1-bit full adder cell, the result is compared with different previous adder logic styles that shows reduction in Delay and Power Delay Product. The results obtained in the proposed work are compared with previous works [4] in terms of area and propagation delay. A reduction in 67.85 % area is obtained as compared to standard CMOS design[8], 43.75 % compared to XOR 4T[4] and 10 % as compared to double pass transistor adder. In terms of delay for all CMOS technologies the proposed adders have least delay as compared to previous designs [4] as shown in Table 3.

The theoretical ideas presented in this article have to be applied to real-world design so as to have less delay and area. In this paper, it has been demonstrated how the delay, power and area has been optimised, which can be employed to create a VLSI chip designing. The approach can been applied to design chip modelling and construction of large and complex micro-controller. This work hopes to be the next step towards further design consideration that need to be employed while chip designing.

9. REFERENCES

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