

Implementation of a Fast and Power Efficient Carry Select Adder using Reversible Gates

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ABSTRACT

All reversible circuits have an intrinsic advantage over traditional irreversible circuits, because they reduce power consumption. Due to this, reversible circuits have been a source of constant excitement and great enthusiasm in the scientific community. Reversible logic is highly useful in nanotechnology, low power design and quantum computing. This paper proposes a design for a faster adder using reversible gates.

Keywords

Reversible Logic, Efficient Adder designs, Carry Select Adder, Power Efficient

1. INTRODUCTION

In a race to come up with faster and more powerful devices, one can observe the unprecedented boom in the digital device design industry. With the advent of new technology, better fabrication techniques and better floor plan designs, devices have become increasingly smaller. The recent advancements in the field of Large Scale Integration, especially over the last ten years have enabled engineers to create new, more powerful devices than ever before. The technology has become ever more portable, personalized and have tremendous built-in functionality. This enhanced processing capability comes at the cost of power loss and power consumption due to increased number of transistors being fabricated into a small area. With the size of the chip being reduced, power consumption has become the paramount concern during design considerations. There is constant research in the field of low power electronics where there is an attempt to find ways to minimize power consumption as much as possible [11].

It is predicted that the Moore's law is at an end due to the inability of the designers to keep up with the power requirements of the future chips [1]. One of the solutions to meet the low-power requirement of the future devices is by adopting an entirely new model known as Reversible Logic. Reversible logic finds its origins in the concepts of Quantum Computing [12]. Researchers like Bennett showed that the devices based on reversible computing consume much less power than the traditional irreversible devices [3, 4]. Reversible logic gates use one-to-one mapping between input and output vectors, thereby preventing loss of information, which in turn results in preventing dissipation of energy, as shown by Landauer [5, 6]. It was proved that $kT \ln(2)$ joule of energy was dissipated at each bit lost. Here k is the Boltzmann constant and T is the temperature. Which meant that a standard (irreversible), three input NAND gate loses up to 2

$kT \ln(2)$ joule of energy each time the circuit is used. This is a considerable power dissipation and can become a nuisance, especially in complex circuits. A large number of circuits (both combinational and sequential) using reversible logic, have been proposed in literature. This paper seeks to implement a faster adder circuits using reversible logic gates.

Toffoli demonstrated in [13] that reversible logic structures are satisfactory for design and implementation in computing structures and organization when those design rules ensure the logic structure is invertible. Deutsch later stated that reversible gates connected to each other by means of unit wires can be sufficiently used for the generation of a quantum computational network [15] [14]. Quantum (reversible) gates are the generalization of classical logic gates. Deutsch defined a source bit of '0' or '1' as a gate which, once every computational step, produces a value of '0' or '1' on its output [15]. He argued that the source bits are reversible gates, since there was a bi-jjective relationship observed between the value produced at the gate input, and the produced output. Since fast computational speed and power efficiency are among the foremost considerations during design considerations, therefore it was the aim of the authors to implement a faster adder (using the carry select scheme).

The paper begins by briefly describing the concept and applications of the reversible logic in section 2. In section 3, the authors have described the concept of reversible logic gates, and have summarized some of the most popular reversible gates. Section 4 of the paper talks about the carry select adder, and its requirement in modern circuits. Further, this section also describes the architecture of the design for a full adder as proposed by the authors. The simulation for the functional correctness of the given circuit is performed in ModelSim and the hardware is described using a Verilog code. Section 5 gives the waveforms generated by the circuit in order to check whether it has been implemented correctly and Section 6 concludes the paper.

2. REVERSIBLE LOGIC

A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments [24]. The most prominent application of reversible logic is found in the generation of quantum computers [22]. Any quantum computer can be considered as a network (or a family of networks) composed of quantum logic gates; therefore each reversible gate is the basic building block for the said network. It has applications in various research areas such as Low Power device design and quantum

computing. Due to the fact that reversible logic has a significant role in reducing power consumption by minimizing the power lost due to individual bit, it has been used to design a gamut of combinational as well as sequential circuits.

Quantum networks have been established to be composed of quantum logic gates; each gate performing a basic elementary unitary operation on one, two or more than two-state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1 [23]. Any unitary operation is reversible and hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible). Thus, quantum arithmetic must be built from reversible logical components [22]. Reversible computation in a system can be performed only when the system comprises of reversible gates. The authors have made use of this principal to create a carry select adder using these reversible gates.

3. BASIC REVERSIBLE GATES

In 1960, researcher R. Landauer demonstrated that circuits using irreversible hardware results in energy dissipation of $kT \ln 2$ Joules due to one bit loss of information where k is Boltzmann's constant and T the absolute temperature [5][6]. Bennett showed that this energy loss can be avoided by constructing circuits using reversible logic gates [3][4]. A reversible logic gate is an n -input, n -output logic function that maintains a one-to-one mapping between the two. Based on this principle, different basic reversible gates such as Feynman [7], Toffoli [8] and Peres [10] have been proposed. A 2×2 Feynman gate with inputs (A,B) produces the output P equal to input A while output Q as the XOR of the inputs [18]. A 3×3 Toffoli gate with inputs (A, B, C) and outputs (P, Q, R). It has outputs P and Q equal to A and B respectively while the output R is complement of the input C if both A and B are at logic 1, otherwise it is input C [21] [19]. A Fredkin gate is a 3×3 gate with inputs A, B and C giving outputs P, Q and R. The outputs are defined as $P = A$; $Q = A'B + AC$; and $R = AB + A'C$ [20]. A Peres gate is a 3×3 reversible gate with inputs (A, B, C) and outputs (P, Q, R). The output P is equal to A; output Q is the XOR of A and B while R is complement of the input C if both A and B are equal to 1, otherwise it is equal to input C [21]. A URG gate is a 3×3 gate with inputs (A, B, C) and outputs $P = (A+B) \text{ xor } C$, $Q = B$, $R = AB \text{ xor } C$ [18].

4. CARRY SELECT ADDER

The carry select adder is a type of adder circuit that is considered more efficient than traditional ripple carry adder.

In fact in a study by R. Uma et al it was found that carry select adders have the least delay out of a wide range of adders [24]. Therefore it was considered as an obvious step by the authors that they propose the design of the fastest possible adder using reversible logic gates. Delays in a circuit may be caused due to a variety of reasons. The primary shortcoming of a ripple carry adder is the fact that at every bit must wait for the result of the previous carry. This is a significant impediment for circuit speed. Each bit waits for the carry generated at the previous bit, in order to calculate the next sum. This causes delays in the circuit. In contrast, the carry select adder, individually calculates the sum and carry for upper and lower bits. For the upper bits it calculates the sum and carry for two cases – when carry propagated from the lower bits is zero as well as for when the carry propagated from the lower bits is one. Then it waits for the carry from the lower bits to reach a multiplexer, where based on the input (whether 0 or 1), the output sum and carry are generated. This significantly improves speed, and reduces delays in the circuit. For an 8 bit number, the carry select adder can be generated as follows.

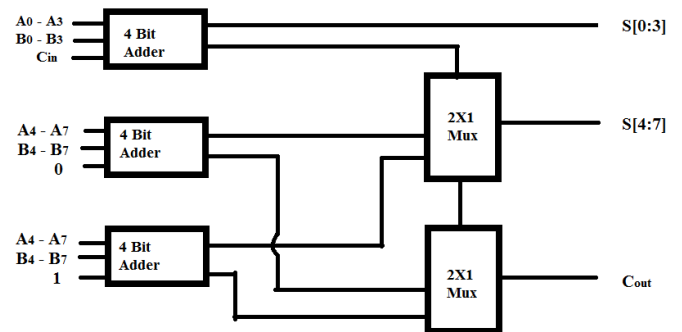


Fig 1: Block Diagram of 8 Bit carry select adder

The above diagram shows how for two 8-Bit numbers A and B, the two numbers were divided into upper and lower bits namely, $A\{0-3\}$ $A\{4-7\}$ and $B\{0-3\}$ $B\{4-7\}$. These have been individually computed, where the lower bits $A\{0-3\}$ and $B\{0-3\}$ have been added along with Carry in (C_{in}). The upper bits namely $A\{3-7\}$ and $B\{3-7\}$ have been computed for both possible values of carry that propagates from the addition of lower bits, namely for carry zero and carry one. A 2×1 Multiplexer decides the value of sum and carry to be used for the upper bits based on the value received from the carry that propagates from the lower bits which it uses as its select line. The implementation of a simple carry select adder for two 2 Bit numbers is given below.

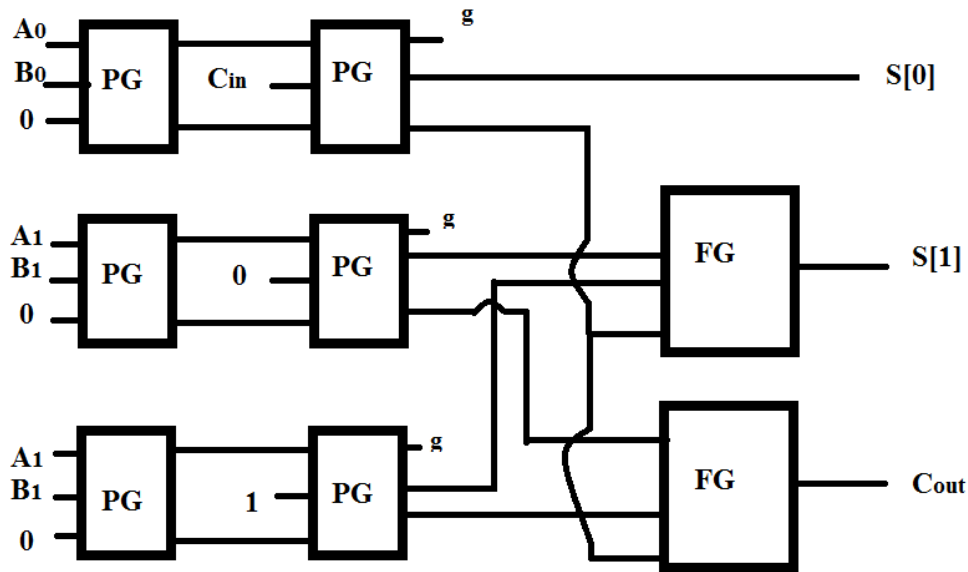


Fig 2: Implementation of a 2 Bit Carry Select Adder using Reversible Gates (Peres Gate and Fredkin Gate)

5. SIMULATION SECTION

The simulation for given implementation was performed using ModelSim tool. The waveform analysis thus generated clearly indicates that the Carry Select Adder worked perfectly for the proposed implementation using Reversible logic gates.

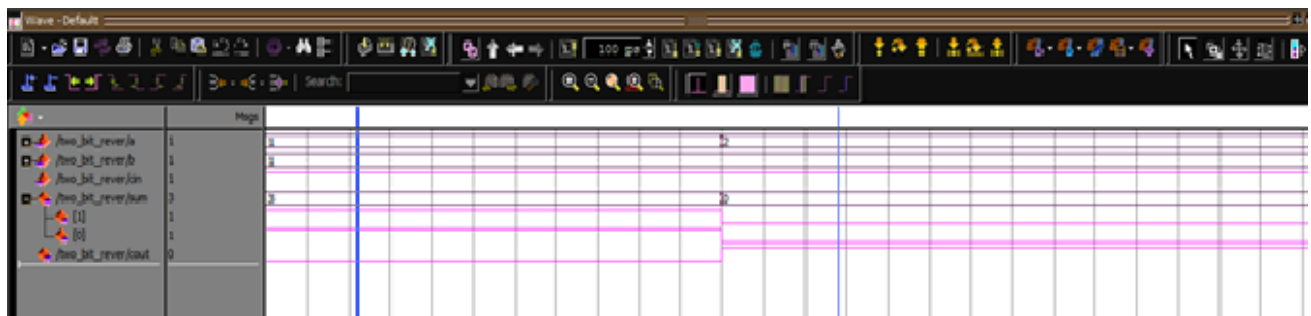


Fig 3: Waveform Synthesis of the circuit of a 2-Bit Carry Select Adder implemented using Reversible Gates

6. CONCLUSION

The proposed reversible logic circuit is an optimized design for basic adders that are fundamental to all computational circuits. With traditional circuits finding difficulty in coping with the increasing processing requirements of the modern technology, reversible logic provides a viable alternative. The designs proposed by the authors can find a wide range of applications in various circuits. With carry select adder providing the least amount of delay and the reversible logic technology providing low power dissipation, the given circuit satisfies two of the most important aspects of digital design. The main goal is to optimize the number of quantum gates, however, they do not address the issue of delay. Although these works do not address sequential circuits, it may be possible to modify and adopt the proposed methods to design reversible sequential circuits. The next future step in the design of reversible sequential circuits is to investigate synthesis of reversible sequential circuits with possibly minimizing or (with minimal) all three metrics of quantum gates, delay and garbage outputs. The proposed designs

will form the basis of efficient reversible sequential circuits to be used in nano-computing regime.

7. REFERENCES

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