An Efficient Processing by using Kogge-Stone High Speed Addition Technique

Rajnish Dubey
M-Tech Scholar
BIST Bhopal
M.P.

Jitendra Jain
Asst. Professor
BIST Bhopal
M.P.

ABSTRACT
In this Technical era the high speed and low area of VLSI chip are very- very essential factors. Day by day number of transistors and other active and passive elements are drastically growing on VLSI chip. All the processors of the devices adders and multipliers are played an important role. Adder is a striking element for the designing of fast multiplier. Ultimately here need a fast adder for high bit addition. In this paper, proposed Kogge-Stone adders are used for binary addition to reduce the size and increase the efficiency or processors speed. Proposing Kogge stone adder provides less components, less path delay and better speed compare to other existing Kogge Stone adder and other adders. Here we are comparing the Kogge Stone adders of different-different word size from other adders. The design and experiment can be done by the aid of Xilinx 14.2i Spartan 3E device family.

General Terms
Ripple carry and Kogge Stone adder, analysis and simulation software tool, Xilinx 14.2i Spartan 3E device.

Keywords
Kogge Stone Adder, Ripple Carry Adder, Proposed Kogge Stone Adder, 14.2i Spartan 3 Device Family.

1. INTRODUCTION
The processors speed mostly depends on adder design techniques. Adder is the device by which two or more than two bit information can be added. For the high speed processing of the data transfer area must be less of the passive and active element. Adder has two outputs specially sum and carry. For making fast adder carry can be reduced and replaced in different ways. The propagation delay or gate delay of a gate is basically the time interval between the application of the input pulse and the occurrence of the resulting output pulse. The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate. The shorter the propagation delay, the higher the speed of the circuit and vice-versa. Propagation delay should be minimizing as possible as, for high efficient addition. For instance 4 bit addition generally propagation delay is occurred highly. When we add one high bit to another high bit carry is occurred due to normally addition operation. This carry propagates to next bit and now bit addition is performed by 3 bit adder. So carry will propagate to the next bit over and over, this cause propagation delay will be occurred. As we have concerned (see in figure 1) (A_3, A_2, A_1, A_0) bits are added with (B_3, B_2, B_1, B_0) then carry propagation delay bits are occurred notations as(C_2, C_1, C_0). On the other hand propagation delay can be reduced by the aid of suitable structural designing process. For instance full adder can be designed with one XOR gate, three AND gate and one OR gate. That type of designing will provide 8.326 ns propagation delay. On the other hand full adder can be design by using two half adder and one OR gate. This type of designing will provide only 8.036 ns propagation delay. Carry propagation delay can be reduced by using ripple carry adder, fast adder that is also called look a-head carry generator, parallel adder, and specially Kogge stone adder.

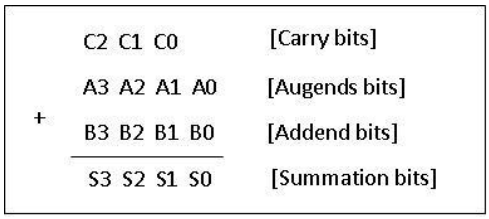

Fig 1: A Propagation delay for four bit binary addition

2. RIPPLE CARRY ADDER
Ripple carry is a combinational circuit for adding more than two bit information. It is also called parallel adder. Ripple carry adder can be designed by using full adder in cascading form. Carry output of first full adder is connected with input of the next full adder, so carry is rippled from one adder to another adder. That is by it is called ripple-carry adder. Let us take example, for designing n bit RCA inputs are $(A_n \dots A_3, A_2, A_1, A_0)$ and $(B_n \dots B_3, B_2, B_1, B_0)$ then carry bits $(C_n \dots C_3, C_2, C_1)$ and summation bits are$(C_{out} \dots S_3, S_2, S_1, S_0)$.

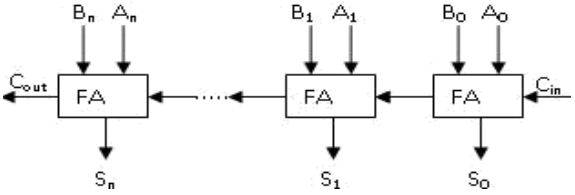

Fig 2: An n-bit Ripple Carry Adder bit binary addition

In this figure all the full adders are connected in cascading form. Carry input C_{in} is an extra input which has fixed value0. First full adder gives the carry output C_1 and summation outputS_0. Carry output of the first full adder is connected with second cascading full adder which will be considered as an input bit.

$$S_0 = (A_0 \oplus B_0) \oplus C_{in} \quad (1)$$

$$S_1 = (A_1 \oplus B_1) \oplus C_1 \quad (2)$$

$$C_{out} = (A_n . B_n) + (C_n . B_n) + (A_n . C_n) \quad (3)$$

3. KOGGE STONE ADDER
Kogge Stone Adder was proposed by Peter M. Kogge and Harold S. Stone. Kogge Stone Adder is an advanced technology of Look a- head Carry Adder. That is also called parallel prefix adder. It has more area than to Brent Kung

Adder but less Fan-out. This adder provides the carry signal time $(O_{logn})$and become fastest adder for industrial level.

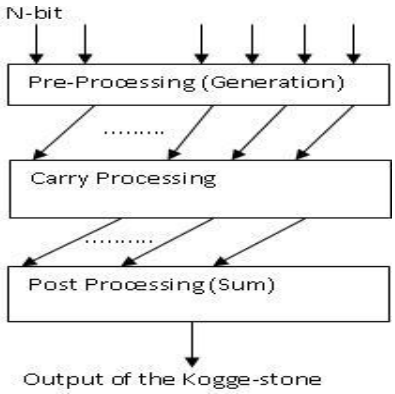

Fig 3: A Block Structure of Kogge Stone Adder bit binary addition

First block of KSA is Pre- Processing that will generate and propagate the carry. Processing of carry will be done over the carry processing area and all the carry signal go through the post processing block. In the pre preprocessing stage we find the, generate and propagate signals from each inputs.

$$P_n = A_n \oplus B_n \quad (4)$$

$$G_n = A_n . B_n \quad (5)$$

Carry processing stage provides the carries corresponding to each bit. Execution of these bit operation is carried out from parallel. After finding the carries in parallel they are segmented in to smaller pieces.

$$CP_{n-1} = P_{n-1} \oplus P_n \quad (6)$$

$$CG_{n-1} = (P_n \oplus G_{n-1}) + G_n \quad (7)$$

Bottom block is summation block which provides the summation bits. That blocks are comprised with XOR gate. If one input is different from another then output will be high. And if inputs are same then outputs will be low. Kogge Stone provides the less area than to other parallel adder like carry select adder, carry save adder and look ahead adder.

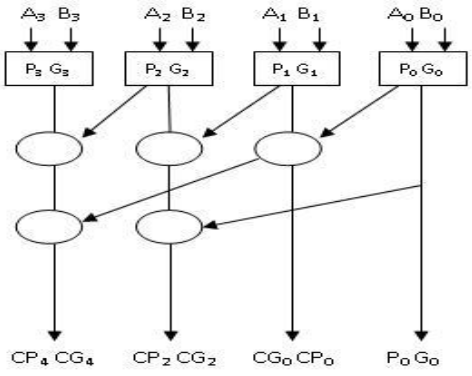

Fig 4: A Functional Diagram of Kogge Stone Adder Stone Adder bit binary addition

Above diagram is a functional diagram of Kogge Stone adder for 4 bit addition. Here elliptically symbol defined as a carry processing stage. The output of the pre processing stage is fed to next carry stage and post processing as well.

4. MODIFIED KOGGE STONE ADDER

The main object of this paper is to reduce the route delay and logic delay. As soon as we increase the bit for addition in Kogge Stone adder area will be increased. So, area and propagation delay can be reduced by the aid of modified KS adder. This adder will be designed like as ripple carry adder. Carry output of one KS adder is connected with another KS adder but this method is very beneficiary for high efficient digital devices as per concerning propagation delay.

$$P = A_i \oplus B_i \quad (8)$$

$$G = A_i . B_i \quad (9)$$

$$C_i = G_i \quad (10)$$

$$S_i = P_i \oplus C_{i-1} \quad (11)$$

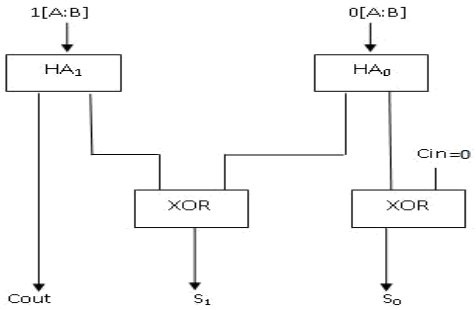

Fig 5: A Modified 2 bit KS Adder

Generally, 2 bit KS adder is comprised with two half adder, two XOR gate. Area of the any circuit is played an important role. Area can be calculated with the help of number of primary gates. Primary gates are AND, OR and NOT. For this type of designing one thing has to be kept in mind C_{in} must be assigned with 0 bit.

5. PROPOSED KS ADDER

Eventually, all the designing levels of digital system or IC's Packages depend on number of gates in a single chip that is also called bottom up approach. Modified KS adder can be reduced regarding the area or number of gates. If we remove the first XOR gate from modified KS adder nothing will be changed for result but area and propagation delay will be reduced.

$$S_i = P_i \quad (12)$$

This equation is applied only for first summation output. For the next sum bit equation will be changed.

$$S_i = P_i \oplus G_{i-1} \quad (13)$$

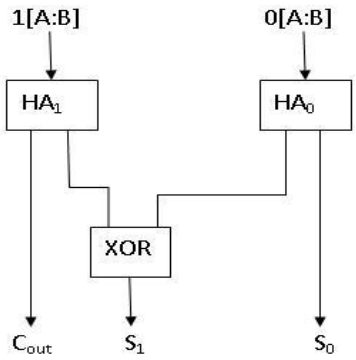

Fig 6: A Proposed 2 bit KS Adder

In above diagram (see in figure 6) $0[A:B]$ defines the inputs A_0 and B_0 which is concerned with HA_0. The first half adder has two outputs sum and carry, S_0 is summation bit for the first half adder and carry output is connected with XOR gate. Output of the XOR gate gives the S_1 output. In the same manner second inputs $1[A:B]$ defines the A_1 and B_1. Last carry is provides the MSB of the output data that is C_{out}.

6. SIMULATION ANALYSIS

Simulation of these experiments can be done by using Xilinx 14.2I VHDL tool. In this paper we are focusing on propagation delay. Propagation delay must be less for better performance of digital circuit. Xilinx is an analysis and simulation tools which has many application in research filed. In this tool simulation is divided in to three categories, model, behavioral and structural. Xilinx 14.2i is an updated version which has many merits than other version.

Table 1: Comparison between different types of adder proposed KS adder

Bit size	Adder	Area	Delay in ns
8 bit	Regular(RCA)	144	11.92
SQRT	BEC	132	13.69
CSLA	Modified (CBL)	111	11.15
	Proposed KS	83	5.776
16 bit	Regular (RCA)	348	16.15
SQRT	BEC	291	18.77
CSLA	Modified (CBL)	276	15.48
	Proposed KS	166	10.85
32 bit	Regular (RCA)	698	28.97
SQRT	BEC	762	34.44
CSLA	Modified (CBL)	552	26.23
	Proposed KS	332	20.56
64 bit	Regular (RCA)	1592	52.82
SQRT	BEC	1498	64.61
CSLA	Modified (CBL)	1104	47.74
	Proposed KS	664	40.25

7. CONCLUSION

Conclusion of this paper is that, designed a low power and less area or minimum propagation delays Kogge Stone Adder. According above table (see Table 1) ripple carry adder and other parallel adder has more number of slices than to propose KSA. Proposing high efficient KS adder can be used for multiplication to design high speed processor. Apart from that it can be used in high speed convolution and de-convolution methods all the experiment has done in Spartan 3E, Xilinx 14.2I VHDL package.

8. FUTURE SCOPE

Now a day's all the devices need a design with compact and high speed portable components. KS adder can used to design a fast multiplier and multiplier is an important device for high speed processor. These devices can be used in high efficient convolution and de-convolution, FIR filter, ALU etc.

9. ACKNOWLEDGMENTS

I would like to thanks to guide, Professor Jitendra Jain Sir who guided with great expertise. And also thanks to ECE deptt who supported on each time. Last but not least my loveable parents and friends who encourage all time.

10. REFERENCES

[1] Soma BhanuTej, 2012.Vedic Algorithms to develop green chips for future, International Journal of Systems, Algorithms and Applications, Volume 2, Issue ICAEM12, ISSN Online: 22772677..

[2] Youngjoon Kim and Lee-Sup Kim, 2001.A low power carry select adder with reduced area,IEEE International Symposium on Circuits and Systems, vol.4, pp.218-221. Tavel, P. 2007 Modeling and Simulation Design. AK Peters Ltd.

[3] Akhilesh Tyagi,1990.A Reduced Area Scheme for Carry-Select Adders,IEEE International Conference on Computer design, pp.255-258..

[4] Belle W.Y.Wei and Clark D.Thompson,1990.Area-Time Optimal Adder Design, IEEE transactions on Computers, vol.39, pp. 666675.

[5] Y. Choi, 2005.Parallel Prefix Adder Design, Proc. 17th IEEE Symposium on Computer Arithmetic, pp 90-98.

[6] Kogge P and Stone H, 1973.A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Relations, IEEE Transactions on Computers, Vol. C-22, No. 8, pp. 786-793.

[7] Madhu Thakur and Javed Ashraf, 2012.Design of Braun Multiplier with Kogge-Stone Adder and Its Implementation on FPGAInternational Journal of Scientific and Engineering Research, Vol. 3, No. 10, pp. 03-06, ISSN 2229-5518.

[8] Pakkiraiah Chakali and Madhu Kumar Patnala , 2013.Design of High Speed Kogge-Stone Based Carry Select Adder, International Journal of Emerging Science and Engineering (IJESE), Vol. 1, No. 4, ISSN: 2319-6378.

[9] Somayeh Babazadeh and Majid Haghparast, 2012.Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit, Journal of Basic and Applied Scientific Research.