Error Detection in 2-bit & 4-bit Multiplier using Parity Predictor Circuit in QCA

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ABSTRACT
Error detection is the detection of errors caused by noise or other impairments during the transmission of signal from transmitter to receiver. Logic design errors may occur during simulation and synthesis due to increase in the complexity of CMOS and VLSI circuits. Error detection method can be either systematic or non-systematic. In systematic method, the transmitter sends the original data unit, and a fixed number of check bits or Parity data is been attached to it, which are derived from the same input data unit. In this work, we describe a method of error detection in 4-bit multiplier with parity predictor circuit in QCA tool. 4-bit multiplier is used as a logic in which we detect error according to its input data. The outputs of logic used and the parity predictor are then compared using comparator. If the values do not match, error has occurred. The technique we used is Concurrent error detection using parity predictor circuit.

Keywords
Error Detection, Systematic scheme, Parity predictor, Comparator, Concurrent Error Detection.

1. INTRODUCTION
In information and coding theory with applications in computer science and telecommunication, error detection and correction or error control are techniques that enable reliable delivery of digital data over unreliable communication channels. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error detection techniques allow detecting such errors, while error correction enables reconstruction of the original data.

Error detection is the detection of errors caused by noise or other impairments during transmission from the transmitter to the receiver. Summer is another name for error detection. Error correction is the detection of errors and reconstruction of the original, error-free data [2].

1.1 Single Bit Error
This type of error occurs when a single-bit of data (such as byte, character or packet) to be transferred, is changed from 0 to 1 or 1 to 0. A single bit error can occur in the presence of white noise.

1.2 Burst/Multiple Bit Error
This type of error occurs when two or more bits in the data stream have changed from 1 to 0 or 0 to 1. Burst errors can be caused by impulse noise. The effects of burst errors are greater at higher data rates.

Redundancy is a form of error detection where each data unit is sent multiple times, i.e. twice. At the receiver side, the two units are compared and if they are same, it I assumed that no transmission errors have occurred. When the data unit is a single character, it is called character redundancy, whereas if the data unit is the entire message, it is called as message redundancy.

2. ERROR DETECTION TECHNIQUES
There are following error detection methods based on redundancy mechanism-

2.1 Vertical Redundancy Check (VRC)
In VRC, a redundant parity bit is introduced to every data unit so that the total number of 1s in data becomes even [9]. Vertical redundancy check is often known as Parity Check, is the most common and least costly process for error detection.

2.2 Longitudinal Redundancy Check (LRC)
A block of bits is sectioned into rows and a redundant row of bits is added to the entire block in LRC. LRC raises the possibility of detecting burst errors.

2.3 Cyclic Redundancy Check (CRC)
CRC depends on binary division. In CRC, in place of adding bits together to get a required parity, a sequence of bits referred as the CRC or the CRC reminder is appended to the end of a unit data. If the reminder is zero, data is accepted otherwise rejected.

2.4 Checksum
The Checksum is used in the internet by several protocols although not at the data link layer. The checksum is based on the concept of redundancy.

Suppose the data is a list of five 4-bit numbers. If the set of numbers is (9, 13, 14, 2, 8), we send (9, 13, 14, 2, 8, 46), where 46 is the sum of original numbers. The receiver adds the five numbers and compares result with the sum. If the two are same, the receiver assumes no error, accepts the five numbers and discards the sum. Otherwise, there is an error and data is not accepted.

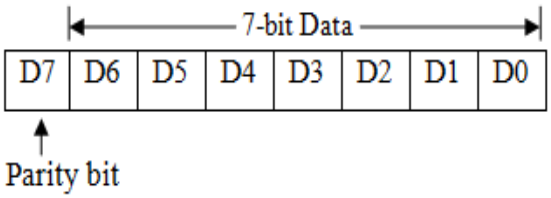

Fig 1: Parity Check

3. CONCURRENT ERROR DETECTION

Concurrent Error Detection (CED) techniques are widely used to enhance system dependability [3].

3.1 General Architecture

Almost all CED techniques function according to the following principle: Let us suppose that the system under consideration realizes a function f and produces output f(i) in response to an input sequence i. A CED scheme generally contains another unit which independently predicts some special characteristic of the system-output f(i) for every input sequence i. Finally, a checker unit checks whether the special characteristic of the output actually produced by the system in response to input sequence i is the same as the one predicted and produces an error signal when a mismatch occurs. Some examples of the characteristics of f(i) are: f(i) itself, its parity, 1's count, 0's count, transition count, etc. The architecture of a general CED scheme (see Figure 2) [11].

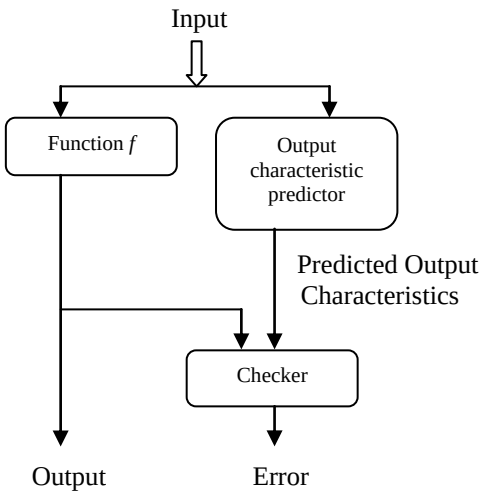

Fig 2: General architecture of a concurrent error detection scheme

3.2 Proposed CED Technique

We have implemented the layout of error detection in 4-bit multiplier in QCA using the block diagram (see Figure 3). In this block diagram, the outputs of our logic (4-bit multiplier) are feed into a parity checker circuit and the inputs of logic are feed to a parity predictor circuit that generates the parity for the data. The predicted parity and the output of checker are then compared to a comparator, that both should be same for the condition of error free logic.

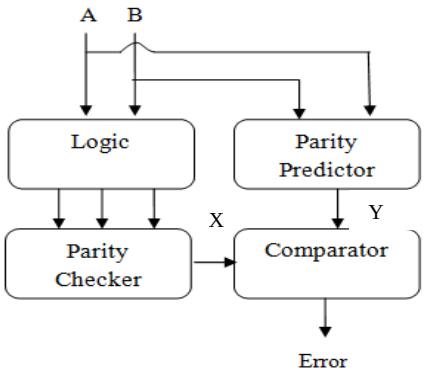

Fig 3: Block diagram of error detection

3.3 Logic Circuit

3.3.1 2 bit multiplier

Here, a 2-bit multiplier module is implemented using two half adder modules (see Figure 4). Very precisely we can state that the total delay is only 2-half adder delays, after final bit products are generated. It is wise to write Implementation Equations of 2x2 multiplier module for simulation [6]. The implementation equations are written as:

R0 (1-bit) = A0.B0

R1 (1-bit) = A1.B0 + A0.B1

R2 (2-bits) = A1.B1 + R1

Product = R2 & R1 & R0

Where '&' denotes concatenation operation.

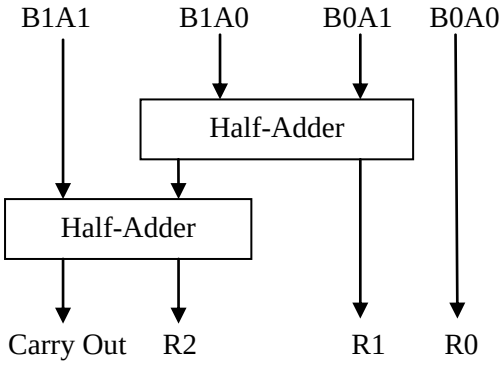

Fig 4: 2-bit multiplier using half adder.

3.3.2 4-bit Multiplier

The implementation of 4-bit multiplier in QCA is done by using 4 half adders and 8 full adders with 16 And-gates (see Figure 5) [1].

3.4 Parity Predictor Circuit

In practice, to detect multiple bit errors, we generate check bits or parity bits from the primary input to compute the checksum for the functional block i.e. 4-bit multiplier [5]. The generated parities and the multiplier functional block outputs are then passed on to the Comparator to generate syndromes that detect the occurrence of error.

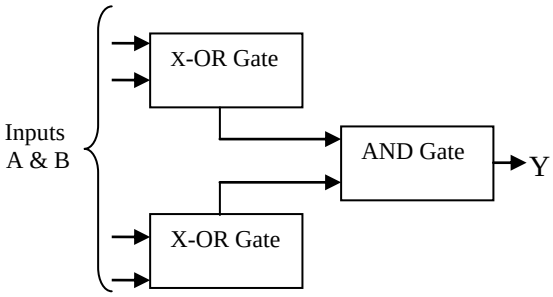

Fig 5: Parity Predictor circuit

3.5 Parity Checker Circuit

A parity predictor and checker circuits is designed using XOR operation. Exclusive-OR functions are very useful in systems using parity bits for error-detection [5]. During transmission of binary signal, a parity bit is used for the purpose of detecting errors. Here we saw how to detect error in logic

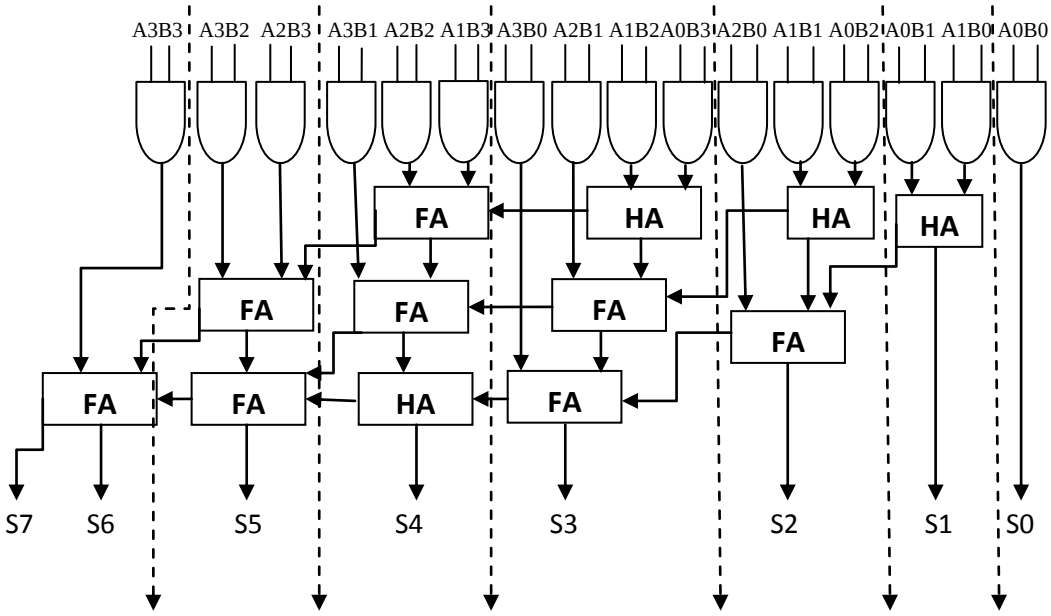

Fig 6: Block diagram of 4-bit multiplier

using parity predictor circuit by implementing blocks in QCA.(see Figure 7)

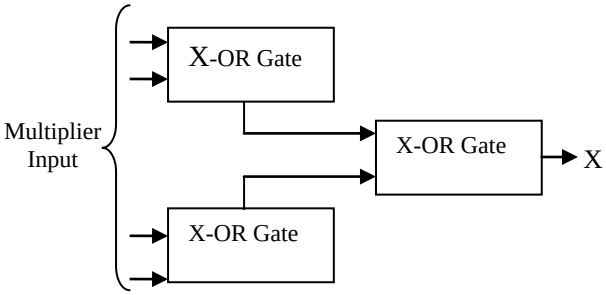

Fig 7: Parity Checker circuit

4. IMPLEMENTATION OF CED IN QCA

Here are the implementations of all circuits in QCA. The Parity Predictor circuit is implemented in QCA having 197 cells and in Area 0.29 um2 (see Figure 8).

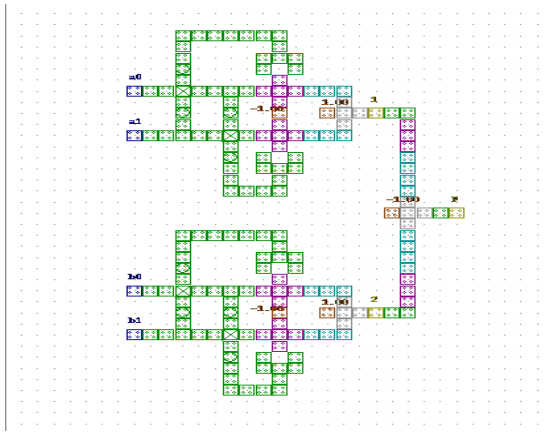

Fig 8: QCA implementation of Parity predictor circuit.

This is a QCA implementation of error detection in 2-bit multiplier using parity predictor circuit.(see Figure 9). In figure, a0, a1, b0 and b1 are inputs of multiplier and m0, m1, m2 and m3 are the product of two bit input, which are then passed to a parity checker circuit (XOR gates). And simultaneously, all the inputs are put into parity predictor circuit whose output must be same as that of the parity checker circuit. If so, then it is an error free circuit. The Area used in implementation of 2-bit Multiplier with error detection layout is 2.28 um2 and total cells used are 1192.

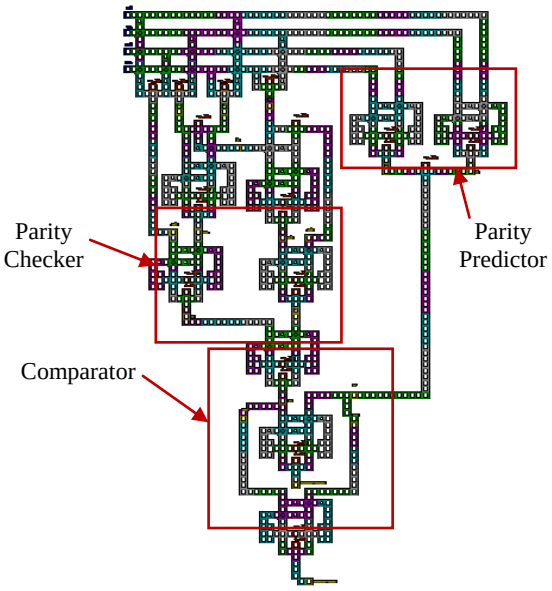

Fig 9: QCA Implementation of error detection logic in 2-bit multiplier

We implemented the layout of error detection in Error detection in 4-bit multiplier in QCA with area 13.95 um2 and number of cells 6349 (see Figure 10).

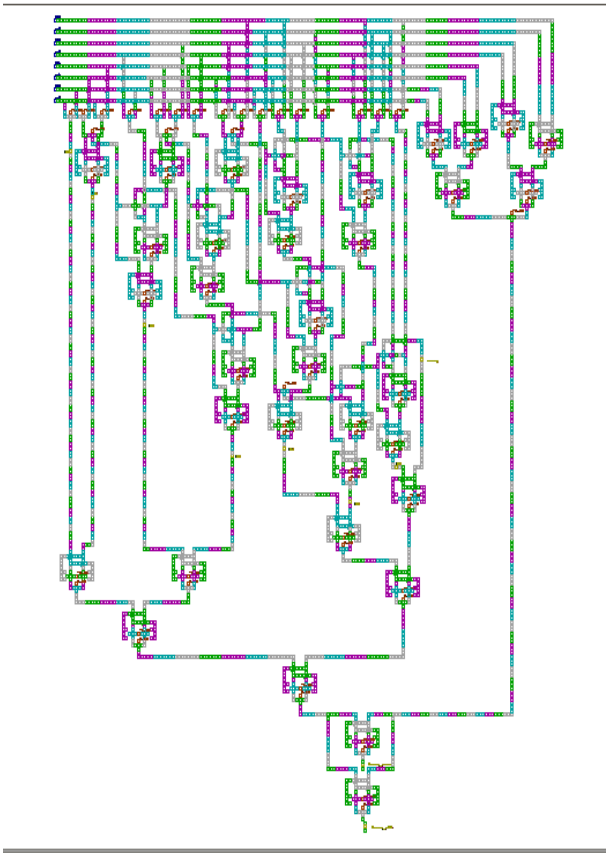

Fig 10: QCA Implementation of error detection logic in 4-bit multiplier

5. SIMULATION RESULTS

Exclusive-OR functions are very useful in systems using bits for error-detection. A parity bit is used for the purpose of detecting errors during transmission of binary signal. Here we saw how to detect error in logic using parity predictor circuit by implementing blocks in QCA. We can say that QCA technology one of the promising nanotechnologies in future that can be used to build arithmetic logic units and microprocessors etc. There are further opportunities for optimization which could lead to densities greater than reported in our present work and could be taken up for further studies. The current QCA technology does not specifically set the possible operating frequency and actual propagation delays, but it can be analyzed as an important parameter in future works [5]. This research work is an attempt to find a reasonable and optimum way of realizing combinational circuit designed from a simple QCA based XOR gate.

Here is the output waveform of error free 2-bit multiplier. The final output i.e. Error is zero, this shows there is no error in the circuit (see Figure 11).

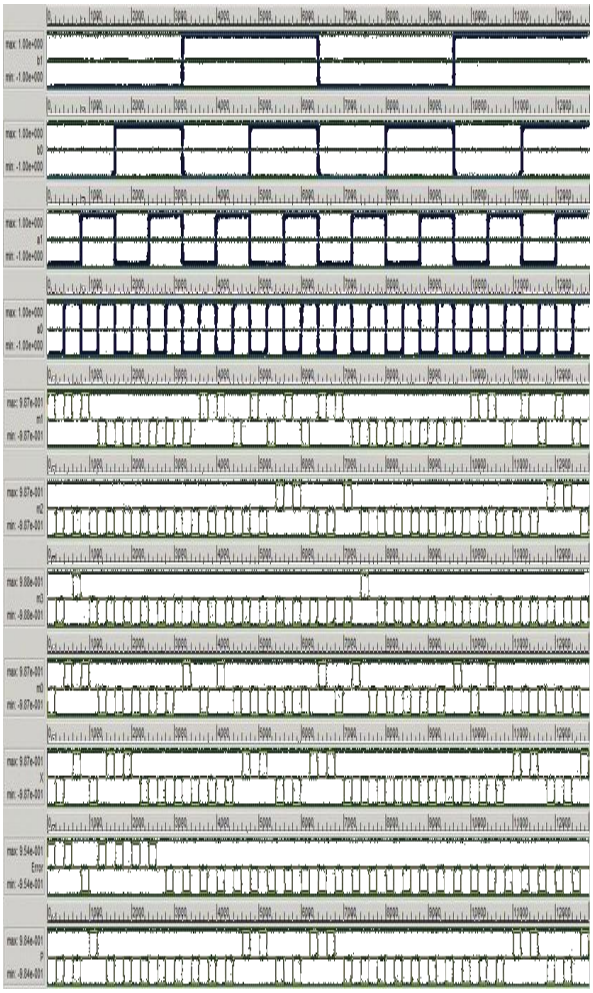

Fig 11: Simulation result of error detection in 2-bit multiplier

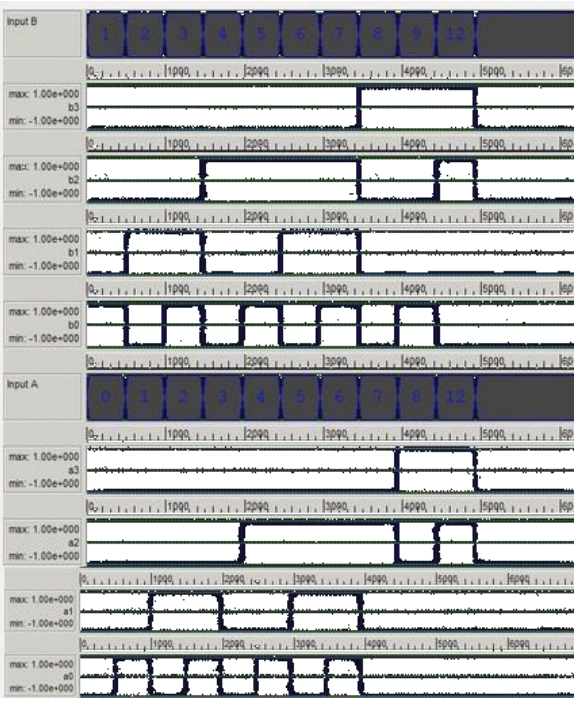

Fig 12: Inputs of 4-bit Multiplier

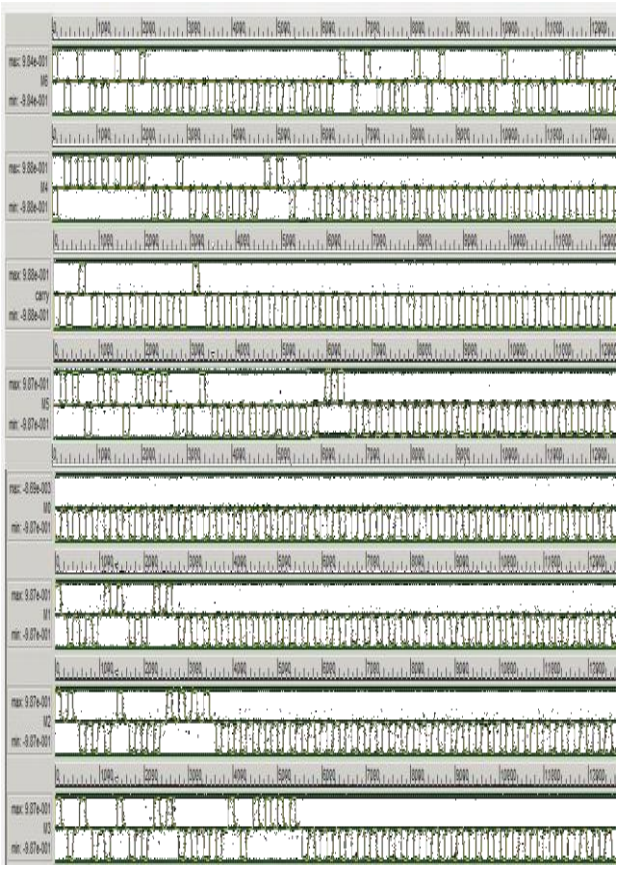

Fig 13: Outputs of 4-bit Multiplier.

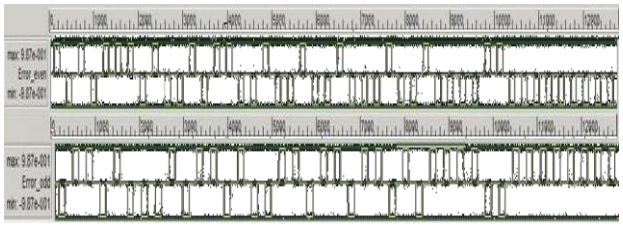

Fig 14: Detected even and odd error outputs of 4-bit Multiplier.

6. CONCLUSION

QCA circuits have significant wire delays. For a fast design in QCA, it is generally necessary to minimize the complexity. his paper presents the design, layout and simulation of combinational circuits based on novel XOR gate configurations. An optional design for XOR based parity predictor and checker circuits are proposed. The proposed layouts were simulated using QCA designer, the design and simulation tool for QCA based circuits. These designs are efficient in terms of cell count, area and power consumption.

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