# Area Efficient High Speed Vedic Multiplier using Common Boolean Logic

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## ABSTRACT
Abstract-In the advanced digital technology the need is of high speed in real time system along with the improvement in implementation issue. Vedic Multipliers has been used to solve the typical and tedious engineering calculation by simple Vedic methods. Here in this paper we have proposed the Vedic multiplier with Common Boolean Logic adder to improve the propagation delay time and area on silicon chip. With this slight improve in the multiplier, great results have been achieved in signal processing tasks. The VM has been designed for the target device XC3S400 -5 PQ208.

## Keywords
FIR filters, Common Boolean Logic (CBL), Vedic Multiplier, Digital Signal Processing.

## 1. INTRODUCTION
Advancement in technology is growing remarkably to sustain the need of smart users. High speed communication and data transfer is the essential requirement of this digital world. High speed of data calculation is the main concern in digital systems. It mainly depends upon the number of gates used to design the logic. Multiplier and adders are the building block in Digital signal processing system. Latency and propagation delays are the area to be worked upon to make the systems efficient with respect to time taken in processing the signal.

Digital multipliers help to achieve the maximum implementation efficiency and clock performance in digital signal processing system. It has fairly large number of circuitry and complex design involved in it. For an example, designing the n bit multiplier the gates used is the square ($n^2$) of input bits.

Multiplication process involves sequence of addition of partial products generated from multiplying the input bits one by one. This process takes large span of time to calculate the result. As the number of bit increases the design of multiplier become more complex to implement. To reduce the processing time the partial product are calculated in parallel simultaneously. Then these partial products have been added with the help of half adder and full adder. A partial product carry is also generated after each addition which has to be added in the next step of addition. The purpose of using this full adder is to reduce the number of additions.

Vedic mathematics is the concept used in the time of ancient Indian and was rediscovered in early twentieth century from ancient Indian sculpture popularly known as Vedas. This Vedic mathematics has been applied to digital algorithm calculations of the digital multiplier. One of the advantages of using Vedic calculation in that it helps in simplifying the complicated lengthy calculation into the simpler forms. Many methods have been proposed for multiplication and division. One generic method is provided for each operation along with some further specific calculations. Urdhwa – Triyakbhyam is the general formula applicable to all cases of multiplication and division. It means vertically and crosswise.

The paper is organized as follows: Section II proposes the related work. Section III contains architecture of proposed Vedic multiplier using carry Boolean logic Section IV provides proposed methodology for Vedic multiplier. Section V contains results and discussion. Section VI conclusions followed by future work.

## 2. RELATED WORK
Laxman P.Thakre et al., [1] proposed Vedic algorithm for the implementation of multipliers to be used in the FFT. The conventional multiplication method requires more time & area on silicon than vedic algorithms. More importantly processing speed increases with the bit length. This will help ultimately to speed up the signal processing task, as it is well known that the multiplier is the basic building block of FFT. The delay of this Vedic Multiplier is 58.28ns and the number of slices used is 461 out of 3584. Number of four input LTUs used is 808 out of 7168.Deepshikha Bharti et al., [2] proposed the design of filter operation with delay efficient addition and multiplication architecture that reduces the bit width. Efficient parallel adder has been used to form FIR filter with 8 and 16 tap. Amina Naaz.S et al.,[3] proposed the efficient multiplier which obtains higher performance for real time signal processing application. It has designed the Vedic multiplier using carry select adder which helps in reducing the delay. This multiplier is implemented to design the parallel FIR filter. Here the propagation delay is 40.38ns and the number of slices used are445 out of 3584. The number of 4 input LUTs are 777 out of 7186.

## 3. COMMON BOOLEAN LOGIC
Area and power efficient high speed data logic path are the most significant areas of research. With the help of simple modification in gate level we can achieve the improvement in the results. Speed of the adder depends on the time required to propagate the carry through the adder. These adder works in series format, that is the sum of the elementary position bit is calculated when the previous bits are summed and the carry is propagated to that next stage.

Carry select adder (CSLA) is one of the advanced adders used in data processing processors to perform fast arithmetic function. It focuses on the problem of carry propagation delay by generating the carry independently at each stage and the select the efficient one with the help of multiplexer to perform the sum. The conventional CLSA is RCA (Ripple carry adder) which generate the partial sum and carry by using the input carry condition Cin=0 and Cin=1, select one out of each pair to form final sum and final carry output. RCA is not area efficient as large number of gates circuitry is used to form the partial products and then the final sum and carry is selected.

Another form of CLSA adder uses binary to excess-1 convertor replacing ripple carry adder with Cin=1. This adder

is known as CLSA along with BEC. The number of gates used has been reduced when we have to design large bit adder. This adders is more conventional as compare to RCA when deal with silicon area used but this is having marginally higher delay time.

## 3.1 Working of CBL

The proposed Common Boolean Logic (CBL) adder is area-power-delay efficient. It work on the logic to remove the redundant adders and use Common Boolean Logic as compare to conventional carry select adder.

The CBL block is comprised of two parts sum generation block and carry generation block. In sum generation block the output sum is achieved using the multiplex. This multiplex is used to select the output value depending on the value of Cin (previous bit). If Cin=0, then output is Xor of the two input bits. If Cin=1, then output get inverted. In carry generation block, multiplexer is used to select the carry of next stage depending upon the previous carry input. If Cin=0, cout is OR of two input and if Cin=1 the output carry is AND of the input bit.

$$If\ C_{in} = 0$$
$$Sum = A\ XOR\ B$$
$$Carry\ A\ OR\ B$$
$$else$$
$$Sum = NOT\ (A\ XOR\ B)$$
$$Carry = A\ AND\ B$$

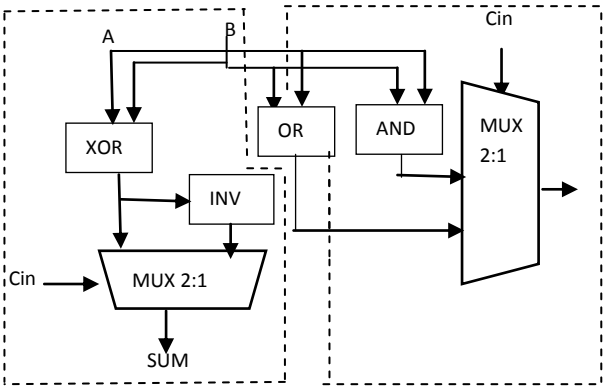



**Figure 1. Block Diagram of Common Boolean Logic Adder**

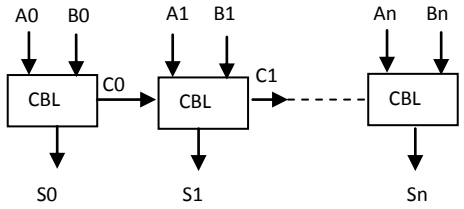



**Figure 2: Block Diagram of n-bit CBL**

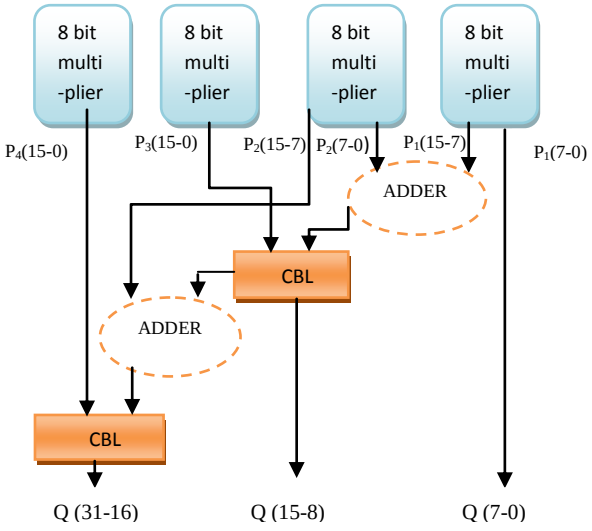
This same process is used for the n number of bits and thus we get the final sum and carry as output.

# 4. PROPOSED ARCHITECTURE OF 16X16 BIT VEDIC MULTIPLIER

The multiplication of two numbers is done by using Urdhwa Triyakbhyam. Here first the least significant bits of the two digits are multiplied. Then the intermediate digits are cross multi-plied and added together. After this the most significant digits are multiplied.

For the 16X16 bit multiplication small block of 2X2 or 4X4 or 8X8 multiplier were used in parallel to make the process easy and efficient.

In our proposed method the high speed carry select adder is replaced by the carry select adder along with Common Boolean logic which claims to provide a better speed and less propagation delay. Here we have used four multiplier of 8 bit to perform 16 bit multiplication. The method used is the addition of all partial product formed by the cross multiplication of one bit with another. The LSB bits of first multiplier P1 (7-0) gives the LSB bits Q (7-0) of the final output. Another bits of first multiplier P1 (15-8) are added in series with LSB 8 bits of second multiplier to form the 16 bits, which in turn get added with 16 bits of third multiplier by using CBL 1 Adder. The LSB bits of the output of CBL 1 adder forms the Q (15-8) bits of the final output. The remaining 8 bit P2(15-8) is then added with the left 8 bits of CBL 1 output to from 16 bits, which is then added with 16 from CBL 2 adder forms the Q (31-16) bits. This is how the 32bit output is achieved in the less possible time.

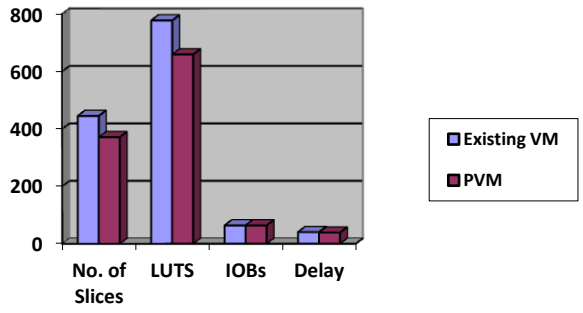


## 5. RESULTS AND DISCUSSIONS

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISETM (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. ISE 14.1i Xilinx tools permits greater flexibility for designs which leverage embedded processors. The ISE 14.1i Design suite is accompanied by the release of chip scope ProTM 14.1i debug and verification software. By the aid of that software we debug the program easily. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Virtex-4 FX and Virtex-5 LXT and SXT FPGAs. With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing.

**Table 1: Comparison Results of Existing and Proposed Vedic Multiplier**

| XC3S400 -5 PQ208 | Existing Vedic multiplier | Proposed Vedic multiplier |
|---|---|---|
| Delay | 40.83ns | 39.10ns |
| Number of Slices | 445 out of 3584 (12%) | 371 out of 3584 (10%) |
| Number of 4input LUTs | 777 out of 7168(10%) | 659 out of 7168 (9%) |
| Number of bonded IOBs | 64 out of 141 (45%) | 64 out of 141 (45%) |




## 6. CONCLUSION

The proposed 16x16 Vedic multiplier architecture has been designed and synthesized using on Spartan 3 XC3S400 board and is used in parallel FIR filter design. The proposed Vedic

Multiplier with carry select adder is compared with the existing Vedic multiplier using Carry select adder along with Common Boolean Logic and can be inferred that proposed architecture is faster compared to existing Vedic multiplier. In future the proposed multiplier performance parameters can be improved by high level pipelining operations and applied in signal processing applications like image processing and video processing.

## 7. ACKNOWLEDGMENTS

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