Design and Simulation of 2:4 Decoder using Hybrid Set-MOS Technology

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ABSTRACT
Single Electron Transistor (SET) is an advanced technology for future low power VLSI devices. SET has high integration density and a low power consumption device. While building logic circuits that comprise only of SETs, it is observed that the gate voltage at the input must be higher than the power supply of SET for better switching characteristics. This limitation of SET in the power and gate supply voltages makes it practically inappropriate to build circuits. An approach to overcome this problem, hybridization of SET and CMOS transistor is implemented. In this paper, different types of hybrid SET-MOS circuits are designed such as inverter and NAND gate and by using above two circuits, 2:4 hybrid SET-MOS decoder is designed and implemented. All the circuits are verified by means of PSpice simulation software version 16.5.

Keywords
Single Electron Transistor (SET), CMOS, Coulomb Blockade, Orthodox Theory, Hybrid SET-MOS, Decoder, Pspice

1. INTRODUCTION
Due to continuous reduction of the physical dimensions of transistor towards the nanometer scale as per the trend of Moore's law, it is obvious that in the near future it would be impossible for further reduction due to quantum effects. The minimum feature size in an integrated circuit has reduced from >1 μm in 1970 to ~ 20 nm in 2013, and it is expected that by 2021, it may be possible to define features smaller than ~ 10 nm (International Technology Roadmap for Semiconductors, 2013).The devices which exhibit charging effects including Coulomb blockade are referred to as single-electron devices. A SET circuit operating in the SET regime can have the smallest available transition time 10^{-15} s, the lowest possible power consumption (working with just a few electrons at μV or mV voltage ranges) and it can have the highest achievable voltage gain. A SET circuit operating in the SET regime can even obtain a switching time in the order of 10^{-15} s, while in CMOS technology the switching speeds are predicted to be on the order of 10^{-10} s and is probably never able to compete to the switching speed values of SET technology.

1.1 Theory of Single Electron Transistor
The principle of operation of SET devices is based on electron tunneling through a nanoscale junction (Fig. 1). The electrons tunnels through the channel one-by-one due to its particular architecture that includes two tunneling junctions [1], [2] and one conductive island [3]. If the charging energy associated with adding the electrons to the island is overcome then only electrons can tunnel onto the island [4].

1.1.1 Orthodox Theory
The 'Orthodox' theory of single-electron tunneling, describes an important charging effect such as Coulomb blockade and Coulomb oscillation [5]. Later this theory revised by Likharev [6]. The orthodox theory makes the following approximations:

1. The quantization of electronic energy inside the conductors is ignored, i.e. the electron energy spectrum is treated as continuous.
2. Time for electron tunneling through the barrier is assumed to be negligibly small ($T_t \sim 10^{-15}$ s) in comparison with other time scales (including the interval between neighboring tunneling events).
3. Cotunneling events are ignored. This assumption is valid if the resistance R_T of the tunnel barriers of the system is much higher than the quantum unit of resistance R_Q.

$$R_T = R_Q, R_Q = \frac{h}{e^2} \approx 25.8\ k\Omega \qquad (1)$$

This assumption is valid only when the electrons are well localized in the island. However, in quantum mechanics it is uncertain. According to Heisenberg's energy uncertainty (ΔE) principle,

$$\Delta E \Delta t > h \qquad (2)$$

where h is plank's constant and Δt is the quantum uncertainity.

1.1.2 Coulomb Blockade Effects
The Coulomb blockade or single-electron charging effect [4], [6], which allows for the precise control of small numbers of electrons, provides an alternative operating principle for nanometer-scale devices. In addition, the reduction in the number of electrons in a switching transition greatly reduces circuit power dissipation, raising the possibility of even higher levels of circuit integration. The SET uses this effect to control the charging of a small 'island' electrode by electrons one at a time [7]. Fig. 2 showed a basic SET, where an island electrode is isolated from source and drain electrodes by tunneling potential barriers with capacitance C_S and C_D. A gate electrode couples to the island electro statically via the gate capacitance C_G and C_G is used to modulate the generated current.

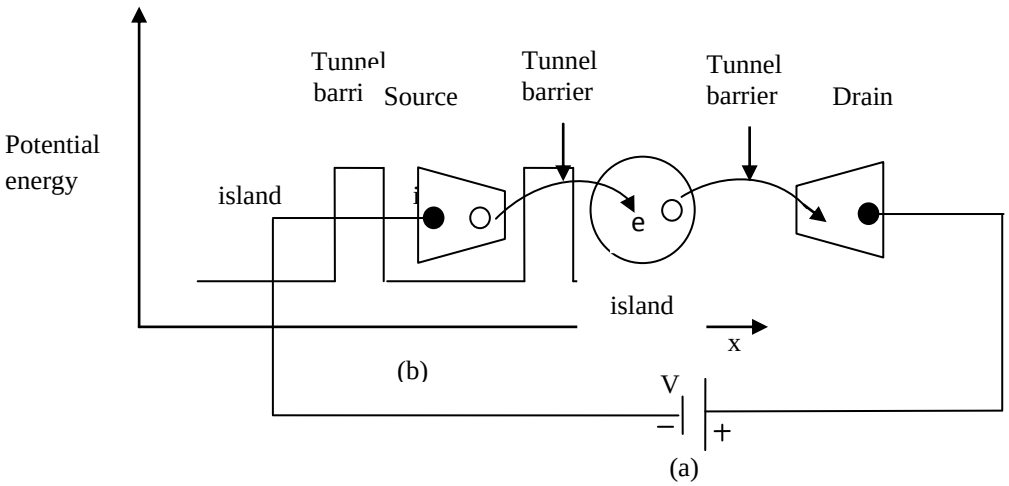

Fig. 1: The single-island, double tunnel junction system (a) Schematic diagram, (b) The potential energy across the system, at zero bias

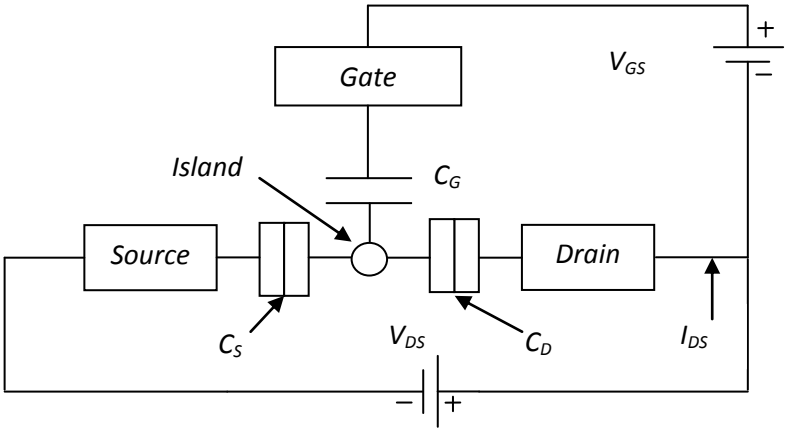

Fig. 2: Circuit diagram of single-island double tunnel junction SET

The charging energy of the system is defined as:

$$E_C = \frac{e^2}{2C_\Sigma} \quad (3)$$

where e is the charge of an electron and C_Σ is the capacitance of this system (C_Σ = C_S+C_D+C_G), associated with a single electron prevents sequential tunneling through the island below a threshold voltage, V_{th} which can be controlled by applying a voltage V_g to the gate. The threshold voltage, V_{th} is the minimum value required for tunneling as shown below [8]:

$$V_{th} = \frac{E_C}{e} = \frac{e}{2C_\Sigma} \quad (4)$$

E_C is the charging energy of the system. As long as the threshold voltage is not reached the junction is blocked.

In order to observe coulomb blockade effects, there are two necessary conditions. One condition is that the charging energy E_C of single excess electron on a quantum dot is much greater than the thermal energy [9], [10].

$$E_C = \frac{e^2}{2C_\Sigma} \gg k_B T \quad (5)$$

In the above expressions, k_B is Boltzmann's constant and T is the temperature of the system. From equation 5

$$T < \frac{E_C}{k_B} \quad (6)$$

Here, the Coulomb blockade is effective at this temperature. The other condition is that the tunneling resistance, R_T of the tunneling junction must be larger than quantum resistance [9].

$$R_T \gg R_Q = \frac{h}{e^2} \approx 25.8\ k\Omega \quad (7)$$

where h is Planck's constant and R_Q is the quantum resistance.

Based on the Coulomb blockade effects, many interesting devices are possible such as precise current standards, very sensitive electrometers, logic gates and memories with ultra low power consumption, down scalability to atomic dimensions, and high speed operation [8]. Therefore, these effects are experimentally verifiable only for very small high-resistance tunnel junctions, meaning small particles with small capacitances and at very low temperatures. Different modeling and simulation techniques Macro modeling of SET [11], Monte Carlo method [9], [12], [13] and SIMON [9] are used for efficient circuit simulation SET.

1.2 Single-electron Transistor Logic

The circuit of the basic quasi-CMOS inverter is shown below in Fig. 3. The quasi-MOSFET surrounded by the dotted line is composed of two tunnel junctions and two conventional capacitors. In this quasi-MOSFET, the functions of quasi-n-MOSFET and quasi-p-MOSFET are switched by simply changing the second gate bias voltage. In the quasi-CMOS

inverter, the output voltage is proportional to the charge stored in the capacitor C_L [14].

SET based inverter which consists of two nominally identical Single-Electron Transistors (SETs) in series that share a common input gate [15]. Each single-electron transistor used in this inverter contains a small aluminum island with a total capacitance $C_\Sigma = 1.6$ fF. On comparison of hybrid SET-MOS inverter [16] and inverter composed of pure SET [15], the voltage gain of hybrid SET-MOS inverter (Fig. 4) has been greatly enhanced. Propagation delay time is further reduced, and the power dissipation has also been reduced notably [17].

Based on the hybrid SET-MOS inverter design [16], of a 2-input NAND gate (Fig. 5) using two series connected SET and depletion type NMOS stage.

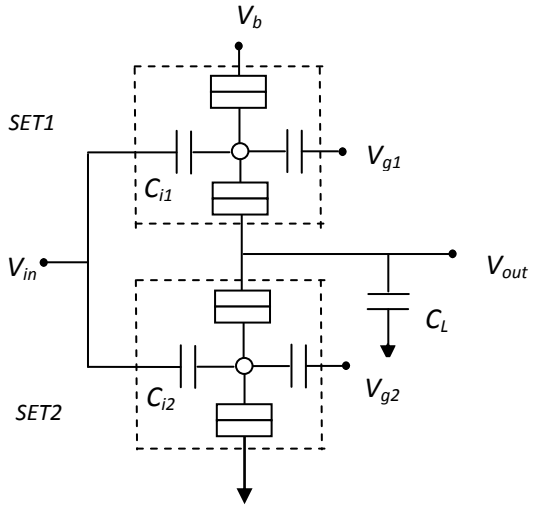

Fig. 3: The basic circuit of the basic inverter

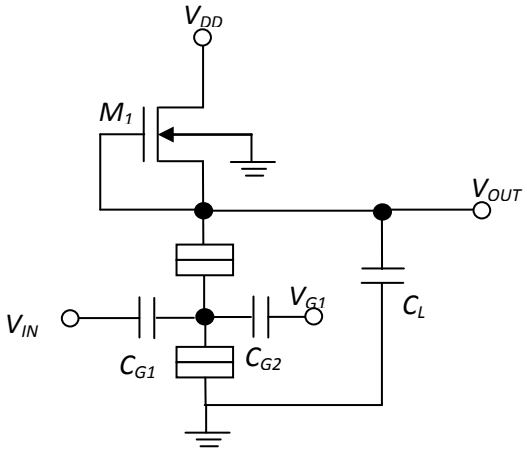

Fig. 4: Equivalent circuit of the inverter using SET and depletion type NMOS transistor

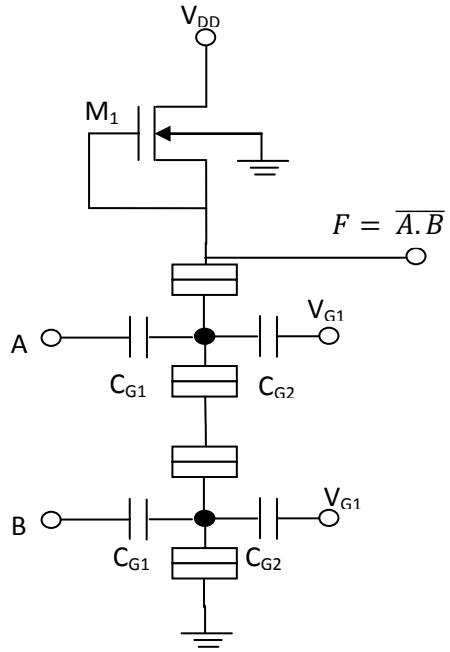

Fig. 5: 2-Input NAND gate using SET and NMOS pull-up stage

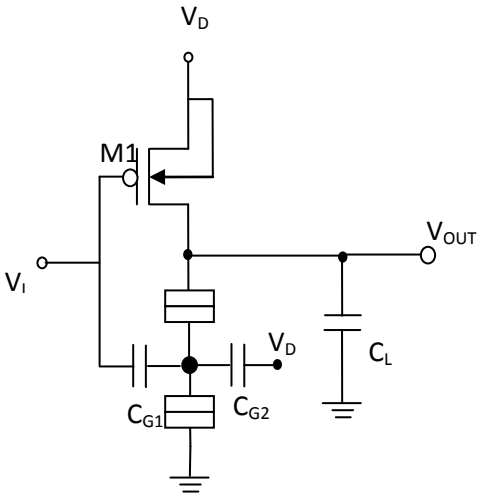

Fig. 6: Circuit of Hybrid SET-CMOS Inverter. V_I is the input voltage and V_{OUT} is the output voltage

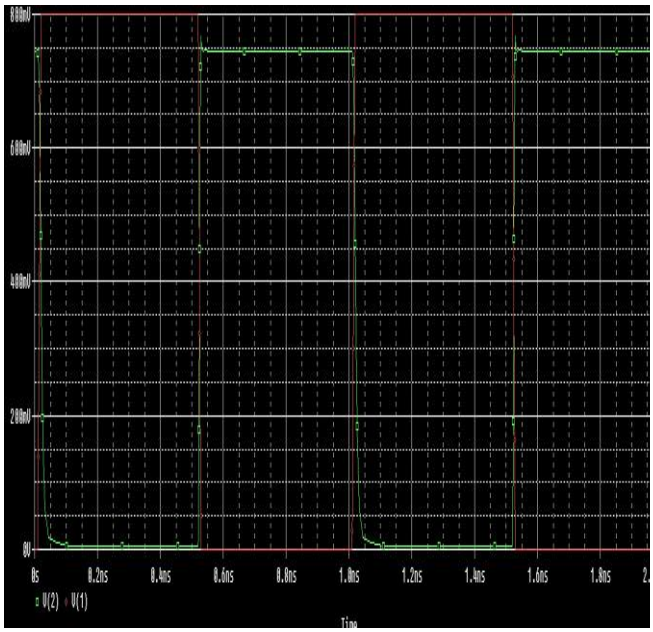

Fig. 7: Output waveform of SET-CMOS inverter

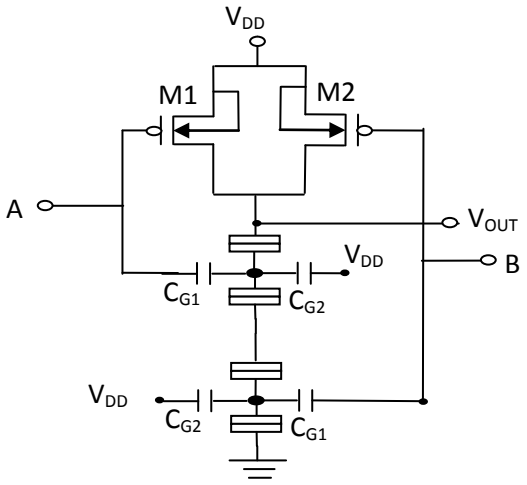

Fig. 8: Proposed circuit diagram of hybrid SET-CMOS NAND gate

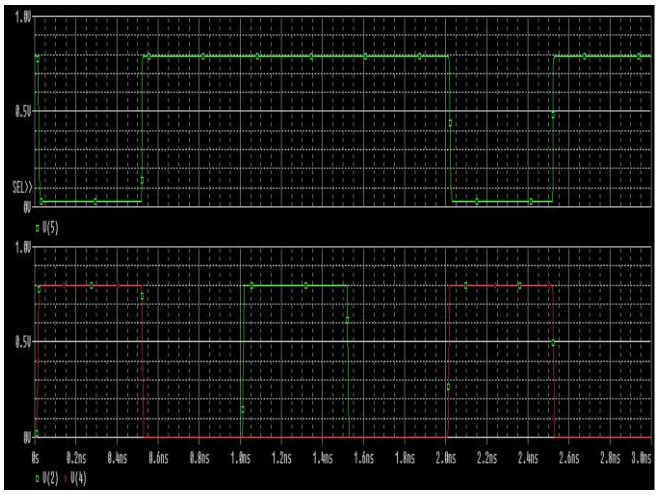

Fig. 9: Output waveform of SET-CMOS NAND gate

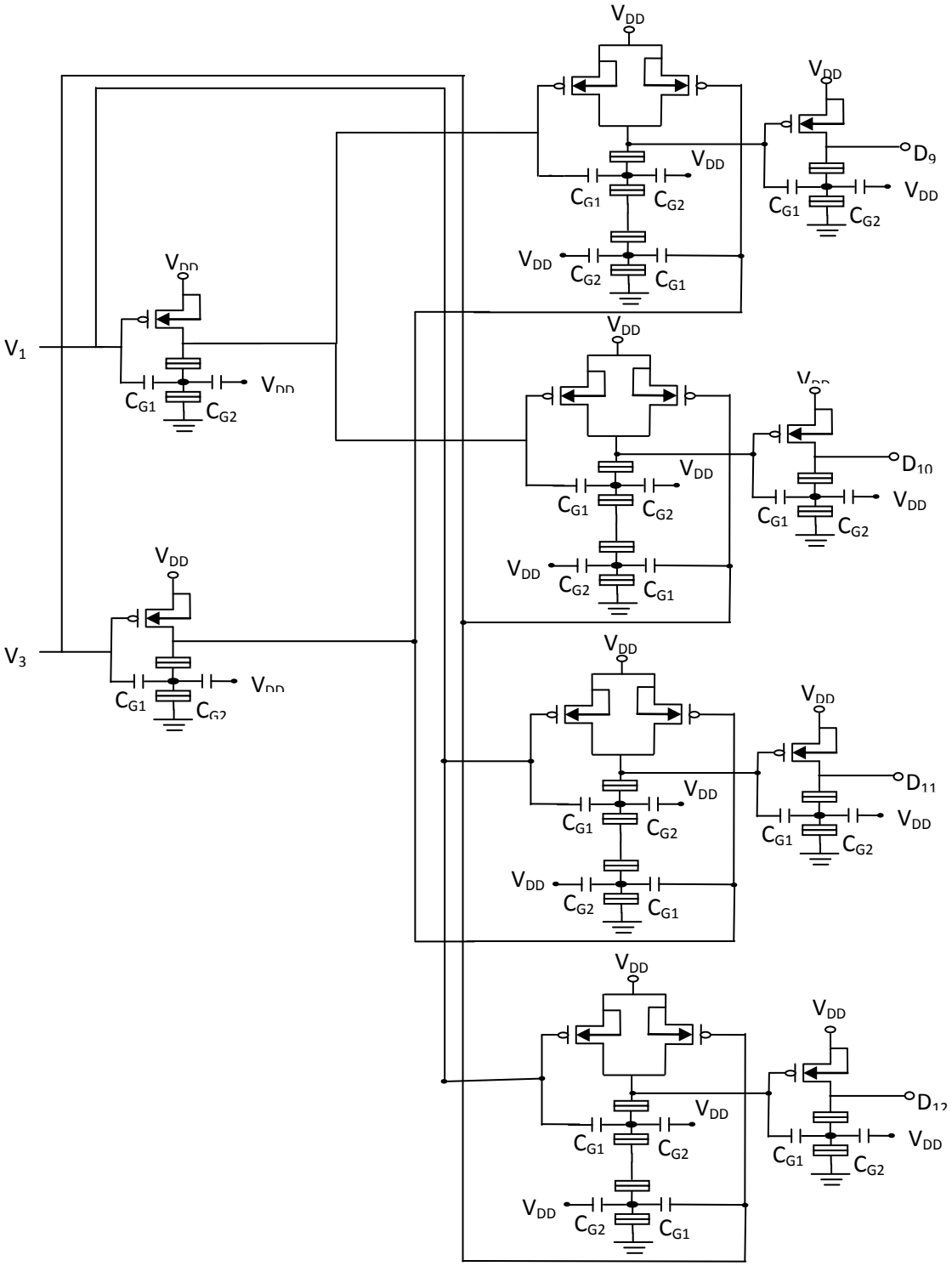

Fig. 10: Circuit design of Hybrid SET-MOS 2:4 Decoder

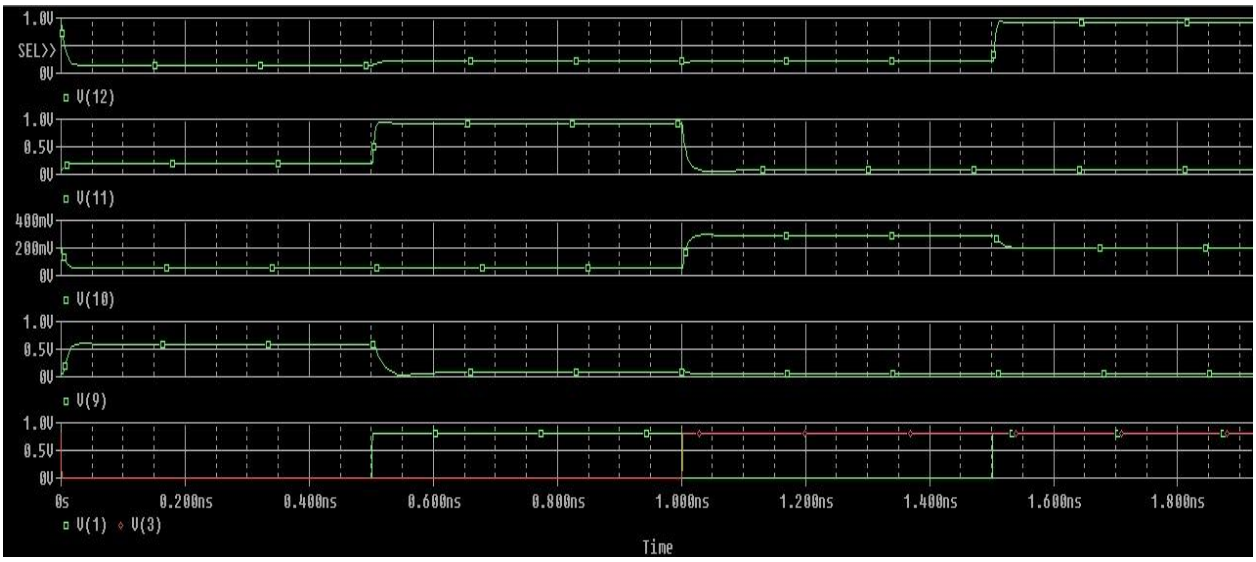

Fig. 11: Simulation results of Hybrid SET-MOS decoder

Table 1: Values of parameters used in simulation

Device	Parameters	Voltage level
SET	$R_1 = R_2 = .1M\Omega$, $C_1 = C_2 = 1aF$, $C_{G1} = 1aF$, $C_{G2} = 0aF$	Logic 0 = '0' Logic 1 = '1' V_{DD} = 0.8V
PMOS	$V_{TO} = 10mV$, $K_P = 10^{-4}$ A/V^2	

2. PROPOSED HYBRID CIRCUITS

2.1 Hybrid SET-CMOS inverter proposed

Hybrid SET-CMOS Inverter which is formed by a PMOS transistor as the load resistance of an SET and the pull down transistor is an SET. Since the MIB model is valid for $|V_{DD}| \leq 3e/C_{\Sigma}$ for single/multiple gate(s) and symmetric or asymmetric SET devices, the bias voltage is taken as 800mV (Fig. 6). The values of the tunnel junction capacitors (C_{j1} and C_{j2}) have been designed to prevent tunneling due to thermal energy.

In above Fig. 6 when V_I = 0.8V (HIGH) then transistor M1 (PMOS) is OFF and SET having both the gate voltages at 0.8V (V_{DD}) is ON then V_{OUT} is 0V (LOW). When V_I = 0V then transistor M1 is ON and SET is OFF, the V_{OUT} is 0.8V (HIGH). So it works as inverter (Fig. 7).

2.2 Hybrid SET-CMOS NAND proposed

In Fig. 8 hybrid SET-CMOS NAND is designed using parameters with $C_{G1} = C_{G2}$ = 1aF and V_{DD} = 8mV. When A = B = 0V then V_{GS} of M1 will be 0V and also V_{GS} of M2 will be 0V. Since the gate voltages are less with respect to sources, both M1 and M2 are ON. Since the gate voltage of SET1 is at 0V and SET2 is equal to 0V, both SETs are OFF. With SET1 and SET2 OFF, V_{OUT} is connected to V_{DD} via M1/M2 and the output is high. When A = 0V and B = 0.8V then V_{GS} of M1 will be 0V and also V_{GS} of M2 will be 0.8V. Therefore M1 is ON and M2 is OFF. Since the gate voltage of SET1 is equal to 0V and SET2 is equal to 0.8 V, SET1 is OFF and SET2 is ON. V_{OUT} is connected to V_{DD} via M1 and the output is high. When A = 0.8V and B = 0V then V_{GS} of M1 will be 0.8V and also V_{GS} of M2 will be 0V. Therefore M1 is OFF and M2 is ON. Since the gate voltage of SET1 is equal to 0.8V and SET2 is equal to 0V, SET1 is ON and SET2 is OFF. V_{OUT} is connected to V_{DD} via M2 and the output is high. When A = 0.8V and B = 0.8V then V_{GS} of M1 will be 0.8V and also V_{GS} of M2 will be 0.8V. Therefore M1 is OFF and M2 is OFF. Since the gate voltage of SET1 is equal to 0.8V and SET2 is equal to 0.8V, both the SET1 is ON. V_{OUT} is connected to V_{DD} via M2 and the output is low (Fig. 9).

All the above circuits are simulated in Pspice taking parameters $C_{G1} = C_{G2}$ = 1 aF and V_{DD} = 0.8 V and for PMOS taking $K_{PO} = 10^{-4}$ A/V^2, V_{TO} = 0.01V.

3. PROPOSED CIRCUIT OF HYBRID SET-MOS BASED 2:4 BINARY DECODER

Binary decoders are another type of digital logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an *n*-bit code, and therefore it will be possible to represent 2^n possible outputs. The proposed circuits are simulated using the software Pspice using the bias voltage is V_{DD} = 0.8 V and the resistor is $100k\Omega$ (Fig. 10). For the PMOS bias transistor, the transconductance was specified with the SPICE parameter $K_P = 10^{-4}$ A/V^2 and the threshold voltage was chosen to be V_{TO} = 0.01V. The values of the parameters used in this simulation are given in Table 1. The simulation result of Hybrid SET-MOS 2:4 Decoder is depicted in Fig. 11. V_1 and V_3 are the inputs and D_9, D_{10}, D_{11} and D_{12} are the outputs.

3.1 Output waveform of 2:4 decoder

From Fig. 10, there are two inputs signal V_1 and V_3. When V_1 and V_3 at logic '0' then the output V_9 selected and when V_1 at logic '0'and V_3 at logic '1' then the output V_{10} selected. When V_1 at logic '1'and V_3 at logic '0' then the output V_{11} is selected and when V_1 and V_3 at logic '1' then the output V_{12} is selected (Fig. 11).

4. CONCLUSIONS

This work explains the basic ideas of Single Electron Transistor (SET) & the concept of hybridization with CMOS technology improve the voltage level at output thus high fan-out. Two hybrid SET-MOS based logic gates (NOT, NAND) are also designed and simulated. Based on these circuits hybrid SET-MOS based 2:4 decoder is proposed, designed and simulated. Hybrid SET-MOS circuits increases the integrated density, helps in futuristic growth towards nanotechnology. This technology reduces the power consumption of circuits.

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