Comparative Analysis of Low Leakage SRAM Cell at 32nm Technology

Jaspreet Kaur
Electronics and Communication Engg Section
Yadavindra College of Engineering,
Talwandi Sabo, India

Candy Goyal
Assistant Professor, Electronics and Communication Engg Section
Yadavindra College of Engineering,
Talwandi Sabo, India

ABSTRACT
Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are the most important criteria for the fabrication of DSP systems. Static random access memories (SRAMs) consist of almost 90% of very large scale integrated (VLSI) circuits. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development toward more compact design rules and, consequently, toward higher storage densities. This paper deals with design of low power static random-access memory (RAM) cells and peripheral circuits for standalone RAMs, in 32nm focusing on stable operation and reduced leakage power dissipation. The work is carried out on Tanner Tool version 13 at 32nm technology.

Keywords
SRAM, VLSI, Leakage Power Dissipation, Static Power, Dynamic Power.

1. INTRODUCTION
Semiconductor memory arrays capable of storing large quantities of digital information (binary logic '1' and '0' bits) are essential to all digital systems. SRAM (Static RAM) is random access memory (RAM) that retains data bits in its memory as long as power is being supplied. Therefore SRAM is a type of volatile semiconductor memory. Unlike dynamic RAM (DRAM), bits are stored in cells consisting of a capacitor and a transistor. SRAM cell consists of a bi-stable latching circuitry made of Transistors/MOSFETS to store each bit, therefore, the cell data is kept as long as the power is turned on and it does not have to be periodically refreshed. SRAM is mainly used for the cache memory in microprocessors, laptops & hand held devices due to high speed and low power consumption. The leakage power affects the chip design process. Speed of SRAM and Power consumption should be taken care of for designing a chip. In SRAM the data is lost when the memory is not electrically powered. SRAM is faster and more reliable than the DRAM. Unfortunately, it is much more expensive to produce than DRAM. Due to its high cost, SRAM is often used only as a memory cache. An SRAM is designed for two needs: For a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU.

The second role for SRAM technology is low power applications. In this case, SRAMs are used in most portable equipment because the DRAM refresh current is several orders of magnitude more than the low-power SRAM standby current. Most of industrial and scientific subsystems, automotive electronics, digital cameras, cell phones and synthesizers contain Static RAM.

SRAM is also used in Cable Modems, workstations, routers, personal computers and peripheral equipment, internal CPU caches and external burst mode SRAM caches, hard disk buffers, etc. LCD screens and printers also employ SRAM to hold the image printed or to be displayed. SRAM buffers are also found in CDROM and CDRW drives to buffer track data, which is transferred in blocks instead of single values.

2. TECHNIQUES FOR OPTIMIZATION OF LEAKAGE POWER USING 1-BIT SRAM CELLS
W/L Ratios for PMOS & NMOS

Equation (1) gives the (W/L) ratio for PMOS transistor [20].

$$\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_3} < \frac{\mu_n}{\mu_p}\cdot\frac{2\left(V_{DD}-1.5\,V_{T,n}\right)V_{T,n}}{\left(V_{DD}+V_{T,p}\right)^2} \quad (1)$$

Equation (2) gives the (W/L) ratio for NMOS transistor [20].

$$\frac{k_{n,3}}{k_{n,1}} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} < \frac{2\left(V_{DD}-1.5\,V_{T,n}\right)V_{T,n}}{\left(V_{DD}-2\,V_{T,n}\right)^2}$$

--------- (2)

$W_1 = W_{NMOS} = 5\times L$
$W_3 = W_{ACCESS} = 2.5\times L$

$L = 32nm$
$W_5 = W_{PMOS} = 1.78\times W$
$\mu_n/\mu_p = 2$

From the above equations we get:

$W_{PMOS} = 142nm$
$W_{ACCESS} = 80$ nm
$W_{NMOS} = 160nm$

2.1 Conventional 6T SRAM Cell

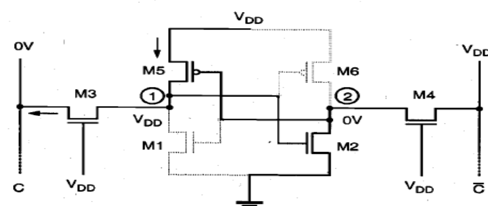

Figure 1.Conventional 6T SRAM Cell

Above Figure shows the write mode of conventional SRAM cell. Word line is used for enabling the access transistors M3 and M4 for write operation.

BL and BLB lines are used to store the data and its compliment. For write operation one bit line is High and the other bit line is on low condition.

For writing "0" BL is High and BLB is low. When we assert the word line high transistor M2 and M4 are ON and any charged stored in the BLB goes through M4- M2 path to ground.

Due to Zero value at Q the M5 transistor is ON and M1 is OFF so the charged stored at Q line.

Similarly in the write "1" operation BLB is high due to this M1 is ON and the charge store on BL is discharged through the M3-M1 path to ground and due to this low value on Q the M6 is ON and M2 is OFF so the charged stored on the QB.

2.2 P-P-N Based Differential 10T SRAM Cell

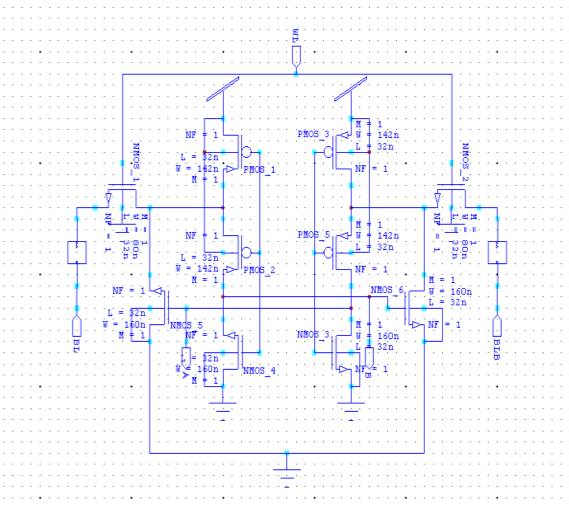

Figure 2. Schematic of P-P-N Based Differential 10T SRAM Cell

As shown in Figure 2. In addition to the standard 6T SRAM cells one extra signal called VGND, denoting a virtual ground signal is added. This cell is called P-P-N based since each of three transistors cascaded in a P-P-N sequence from top to bottom. Stack transistors are connected in pull down paths to reduce power dissipation [2].

2.3 Fully Differential Based 10T SRAM Cell

Design of cell consists series connection of tail transistor, Gate electrode is controlled by output of XOR gate. Tail transistor and XOR gate is shared by all the cells in a row. Inputs are tapped from WWL and RWL. Width of the Tail Transistor is kept large (800nm) in order to Improve Static Noise Margin, resulting in stability [2].

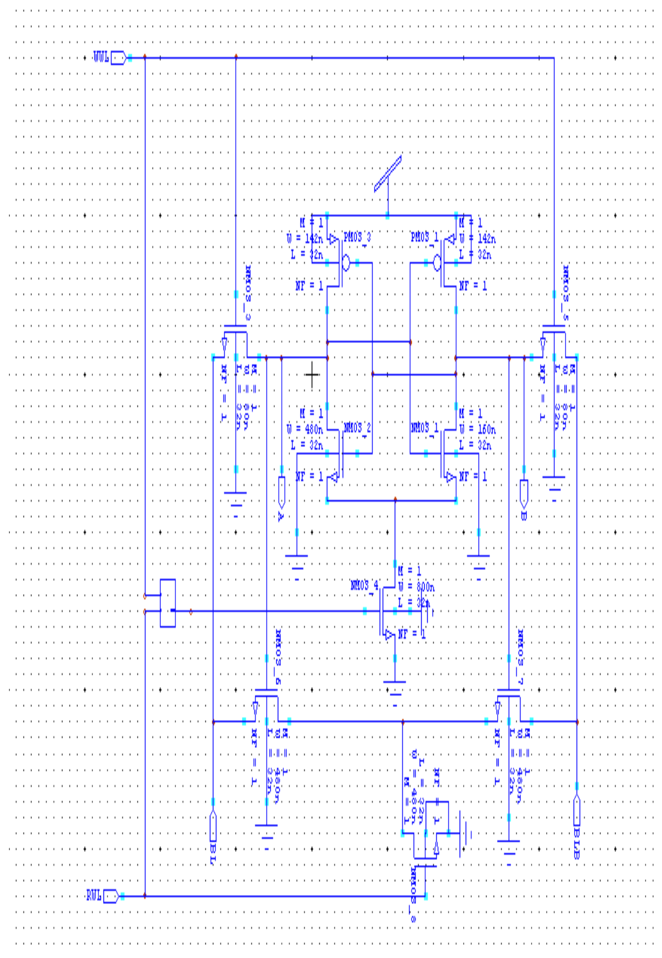

Figure 3. Schematic of Fully Differential Based 10T SRAM Cell

2.4 Anti-leakage Based 10T SRAM Cell

In this low power technique, the decoupling transistor P3, P4 and the anti-leakage transistor P5, P6 reduce the leakage power. The decoder section can also be designed for high V_{th} operation, by which the leakage currents can be reduced [2].

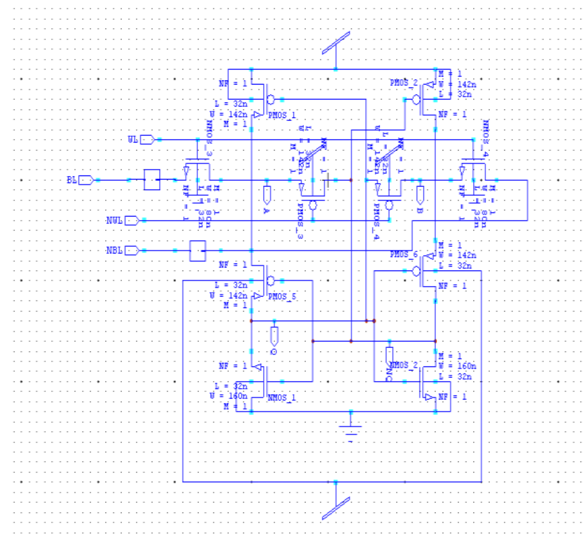

Figure 4.Schematic of Antileakage Based 10T SRAM Cell

3. MODIFIED 1-BIT SRAM CELLS

3.1 NMOS SRAM Cell

The NMOS SRAM Cell has been implemented using two NMOS transistors with the driver transistors as shown in Figure.5.

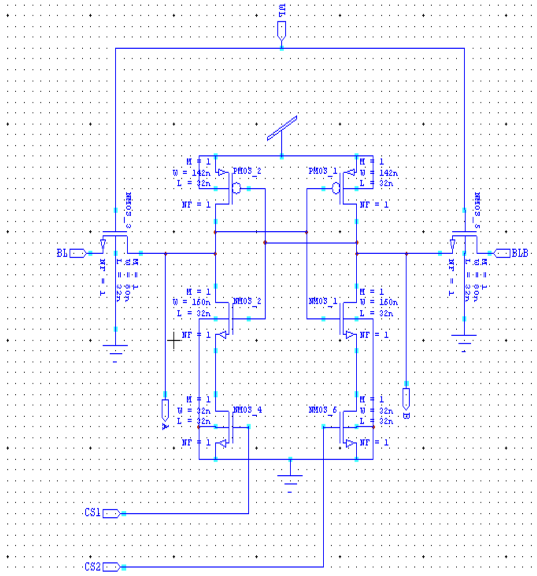

Figure 5. Schematic of Modified 1-BIT NMOS SRAM Cell

3.2 P-NMOS SRAM Cell

The P-NMOS SRAM Cell has been implemented using one PMOS transistor and one NMOS with the driver transistors as shown in Figure.6.

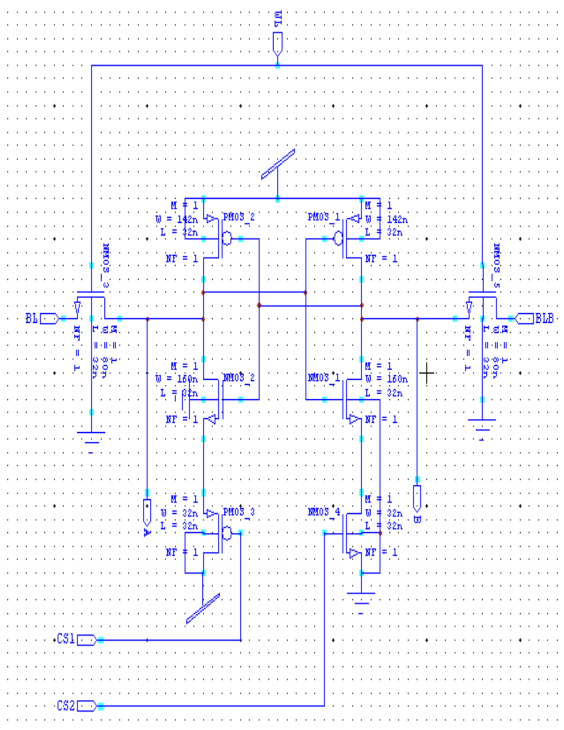

Figure 6. Schematic of Modified 1-BIT P-NMOS SRAM Cell

3.3 N-PMOS SRAM Cell

The N-PMOS SRAM Cell has been implemented using one NMOS transistor and one PMOS with the driver transistors as shown in Figure.6.

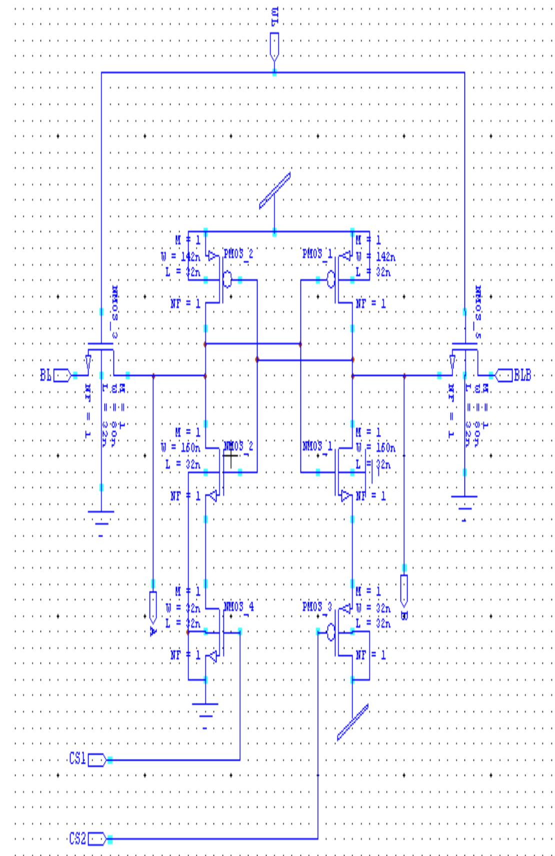

Figure 7. Schematic of Modified 1-BIT N-PMOS SRAM Cell

4. SRAM ARCHITECTURE

Figure 8. Gives an overview of an SRAM memory design for a single data bit input / output. A single address of *N+M* bits is split into N row addresses and M column addresses. The row address is first decoded, so that one out of 2^N word lines in the memory array (of size 2^N x 2^M) is being selected. Most RAMs are built so that all cells in the same row are activated. Consequentially, all 2^M bit line pairs forming the columns leaving the memory array now contain data. The column decoder select one of these line pairs based on the column address. Typically, the signal is sense-amplified, and then put into the data read buffer.

The main SRAM building blocks are as follows.

- SRAM cell
- Pre-Charge Circuit
- Column decoder Circuit
- Sense Amplifier
- Row decoder

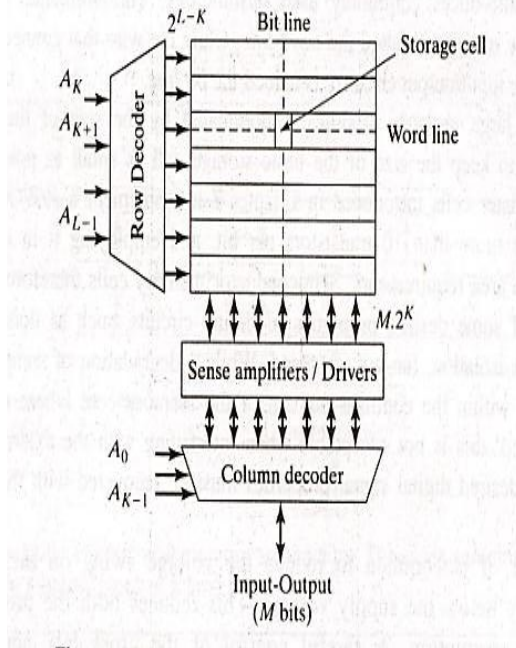

Figure 8. SRAM Architecture

4.1 Pre-Charge Circuit

The pre-charge circuitry brings the BL and BLB to be the same voltage before a read cycle. The simplest version of pre-charge circuitry consists of three transistors that can be either NMOS or PMOS devices. Two of the transistors are used to connect the bit lines to V_{dd}, and the third transistor is connected between the two bit lines to ensure that the lines end up being the same voltage. To pre-charge the bit lines, the signal PRE is brought to logic 0. This turns on all three transistors which then charge and equalize BL and BLB to be V_{dd}.

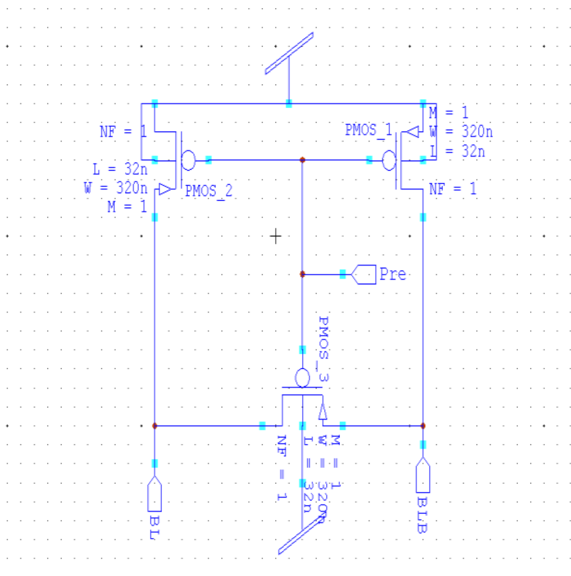

Figure 9. Schematic of Pre-Charge Circuit

4.2 Column/Row Decoder

A decoder has 16-line de-multiplexing capability which decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs.

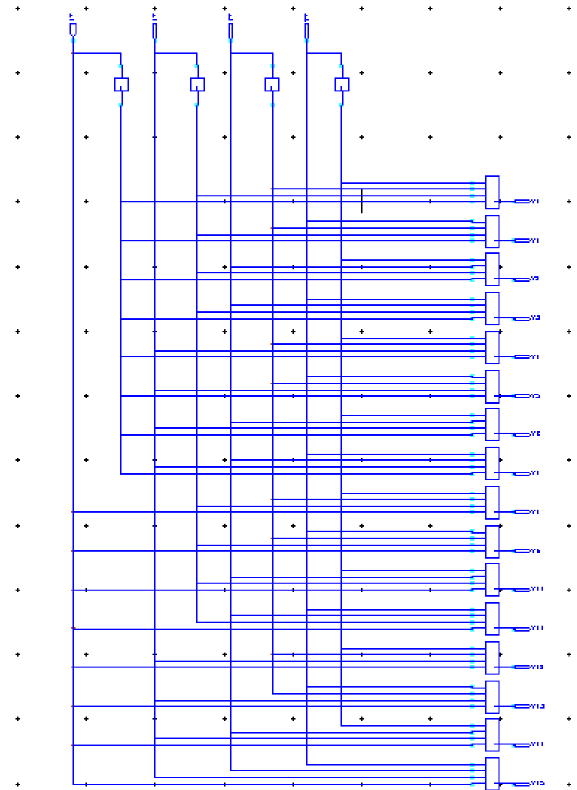

Figure 10. Schematic of 4x16 Decoder Circuit

4.3 Sense Amplifier Circuit

The sense amplifier is in charge of detecting what value is stored in an SRAM cell during a read cycle and displaying that value at the output. Since only one row of data is accessed during each read cycle, each column of cells within the SRAM array requires only one sense amplifier. A sense amplifier works by sensing a relatively small difference between the voltages of the two bit lines, then amplifying the difference at the output to show if a cell is storing either logic 1 or 0. The bit lines are pre-charged before each read cycle to ensure that the difference between the bit line voltages are caused by the value that is stored in the cell. If the bit lines are not pre-charged, there is a chance that the sense amplifier could misread and present an incorrect value at the output.

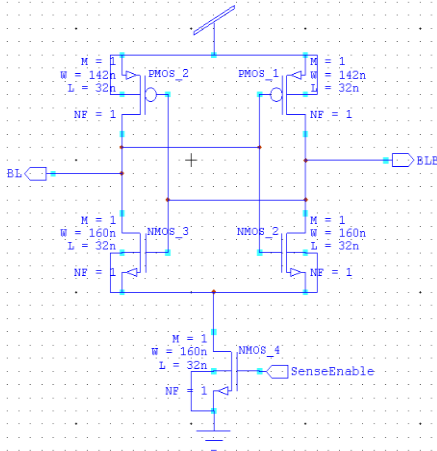

Figure 11. Schematic of Sense Amplifier Circuit

4.4 16x16 SRAM ARRAY

The above 1 Bit building blocks are used to design the 16x16 SRAM Array.

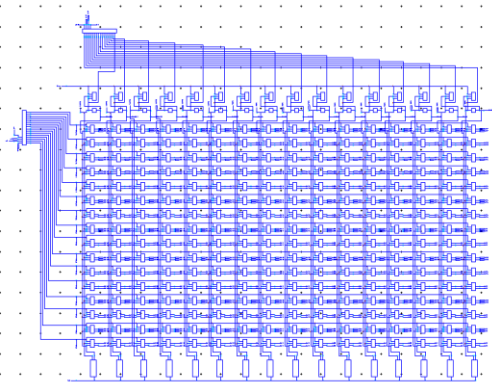

Figure 12 a. 6T SRAM 16x16 Array

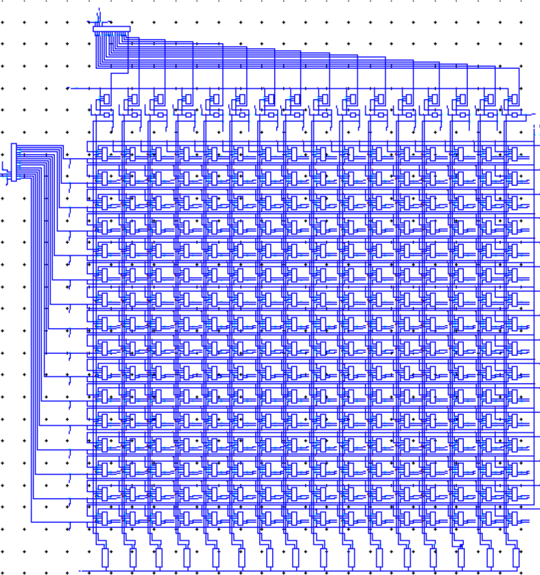

Figure 12.b Modified NMOS SRAM 16x16 Array

5. STABILITY

The first consideration in the SRAM cell design is the stability that is the ability to hold a stable cell state.

Static Noise Margin (SNM) is an important parameter in determining the cell stability. The SNM of SRAM cell is defined as the maximum value of noise that can be tolerated by the cross-coupled inverters before altering state.

According to the results shown in the SNM of the conventional SRAM cell (SNM_{conv}) is characterized with the following expressions.

$$SNM_{Conv} = V_T - \frac{1}{k+1} \cdot \left(\frac{V_{DD} - \frac{2r+1}{r+1} V_T}{1 + \frac{r}{k(r+1)}} - \frac{V_{DD} - 2V_T}{1 + k\frac{r}{q} + \sqrt{\frac{r}{q}\left(1 + 2k + \frac{r}{q}k^2\right)}} \right)$$

where

$$\begin{aligned} r &= \beta_{driver}/\beta_{access}; \\ q &= \beta_{load}/\beta_{access}; \\ k &= (r/r+1)\left(\sqrt{(r+1/(r+1-V_s^2/V_r^2))} - 1\right); \\ V_s &= V_{DD} - V_T; \\ V_r &= V_s - r/(r+1)V_T. \end{aligned}$$

β_{driver}, β_{access} and β_{load} are the W/L ratios of driver transistors (N1, N2), load transistors (P1, P2) and access transistors (N3, N4), respectively V_{DD}= 1.0v, V_T=0.4v.

For Fully Differential 10T SRAM Cell the cell ratio of the ZA cell having tail transistor N4 is r'= ($\beta_{N2} \times \beta_{N4}$) / ($\beta_{N1}(\beta_{N2} + \beta_{N4})$). To maintain the ($SNM_{ZA}$) same as the ($SNM_{Conv}$) the cell ratio r' must be equal to the conventional cell ratio r, which can be achieved by appropriate choice of β_{N2} and β_{N4}.

The SNM_{ZA} in different combinations of β_{N2} and β_{N4} when β_{N1} =1 keeping the value of β_{N2} and β_{N4} 3 and 5 (i.e., the conventional cell ratio is fixed to 2).

The ZA cell ratio r'= 15/8 approximates the conventional cell ratio r= 2 that verifies the estimation model developed by Keeping the value of W_{N1}, W_{N2} and W_{N4} (tail transistor) 160nm, 480nm and 800nm.

Case I: Calculation of SNM, without taking the average of the widths of Driver and Load Transistors.

Case II: Calculation of SNM, by taking the average of the widths of Driver and Load Transistors.

Table 1. SNM of 1-Bit SRAM Cells

Sno.	SRAM Cell (1 Bit)	Static Noise Margin (mV) Case I	Static Noise Margin (mV) Case II
1.	Conventional 6T	434	-
2.	PPN 10T	434	421
3.	Fully Differential 10T	437	-
4.	Anti-Leakage 10T	434	436
5.	Modified NMOS	434	427
6.	Modified P-NMOS	434	427
7.	Modified N-PMOS	434	427

6. RESULTS AND COMPARISON

This section provides the detailed simulation analysis of the different 1 bit and 16x16 bit configurations of SRAM cell. The Average Power Dissipations (Static + Dynamic), Delay and Static Noise Margin for SRAM cell are estimated. The schematic of the SRAM cell is designed and implemented by using Tanner Tool V13.Simulation has been done in 32 nm environment with a power supply of 1.0 volt and at an operating frequency of 500MHz.

The simulation results for 1 Bit and 16x16 Bit SRAM Cells is shown in Table 2 and Table 3 Respectively.

Table 2. Comparison of 1-Bit SRAM Cells in terms of Power & Delay

Sno.	SRAM Cell (1 Bit)	Average Power (µW)	Leakage Power (µW)	Delay (ns)	PDP (fj)
1.	Conventional 6T	2.64	0.20	0.06	0.15
2.	PPN 10T	83.7	78.9	0.63	52.7
3.	Fully Differential 10T	12.0	7.90	0.06	0.72
4.	Anti-Leakage 10T	51.6	0.39	0.09	4.64
5.	Modified NMOS	0.90	0.19	0.05	0.04
6.	Modified P-NMOS	6.27	10.9	0.05	0.31
7.	Modified N-PMOS	6.27	0.16	0.04	0.25

Table 3. Comparison of 16x16 Bit SRAM Cells in terms of Power & Delay

Sno.	SRAM Cell (16x16 Bit)	Average Power (mW)	Leakage Power (mW)	Delay (ns)	PDP (pj)
1.	Conventional 6T	6	5.9	0.29	1.74
2.	PPN 10T	21.5	21.5	0.39	8.38
3.	Fully Differential 10T	12.8	14.3	0.81	10.3
4.	Anti-Leakage 10T	3.95	2.12	0.41	1.61
5.	Modified NMOS	1.79	2.06	0.03	0.05

7. CONCLUSION & FUTURE SCOPE

Low leakage SRAM Cells using Tanner Tool (v.13) is designed in this paper. Three Modified Low Power NMOS SRAM cell has been presented in this work. In the Modified SRAM cell average power dissipation is reduced because of the reduction of switching capacitance. The simulation results shows that the Modified SRAM cell consumes less average power, which is 0.9µW for 1Bit SRAM Cell and 1.79mW for 16x16 Bit SRAM Cells.

Results show that the measured Delay is 0.04ns for 1 Bit SRAM Cell which is having improvement up to 93%, and is having a value of 0.03ns for 16x16 Bit SRAM Cell Array.

Static Noise Margin value of Modified SRAM Cell is 434mV. So, it is concluded that Modified SRAM cell can be used to provide Low Power solution in battery operated devices like mobile phones and laptops etc.

One can extend this work for higher frequency of operation also larger size of SRAM can be the future scope of this paper.

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