

Optimized High Performance 10T SRAM Cell Characterization

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ABSTRACT

In this work, optimized Low power and high speed SRAM architecture based on ten transistor (10T) bit-cell is proposed. This cell obtains low static power and high speed read due to two independent read access mechanisms, which offers cascading of read driver. It also estimates read/write delay, read stability, write stability and compare the result with that of standard 6T, 9T and LP10T SRAM cell. The comparative study based on VDD and Temperature variation using simulation exhibits appreciable improvement in read delay and write SNM.

General Terms

VLSI Circuit

Keywords

Standby Powers, Read Operation Delay, Write Operation Delay, Monte Carlo Simulation and Static Noise Margin.

1. INTRODUCTION

To support faster read and write operations, need large size SRAM Cache memories in multi-core architecture. This large size cache has occupied 90% of total chip area (Montecito processor)[1]. Since the total leakage power is proportional to transistor count and its W/L ratio, a reduction of the SRAM cache leakage is therefore inevitable for low power design. Large sizes of pull-up and pull-down MOS device are responsible for sub-threshold leakage or static power dissipation as well as occupy more area on the total chip area. But large size of pull up and pull down MOS is required for reliable read and write operation. Standard 6T SRAM cell suffer from that problem. As observed in the 8Kbyte instruction cache of the M32R processor at 45nm technology, in idle state leakage power dissipation in SRAM cache can exceed the dynamic power dissipation [2].

The another issue considered in design is to ensure a reasonable noise margin, which is measured in term of Static Noise Margin (SNM) and the Write Trip Point [3], [4]. According to [3], SNM degrade when threshold voltage variation increases. Furthermore, the SNM is linearly dependent on the supply voltage, reducing which to save power has a negative impact on the cell stability. As a result, it is extremely difficult to maintain the cell stability as technology enters the sub-100 nm regime.

For scaled VLSI devices, sub threshold leakage current, junction leakage current and gate leakage current are becoming important leakage component, for applications such

as embedded cache and battery operated systems where leakage currents must be kept extremely low. Therefore, leakage is a serious issue in scaled technology.

A single bit line based 6T SRAM cell [5] offers higher write operation delay. A low power differential 6T SRAM cell [6] provide significant improvement in read operation delay and write power (energy) but can't improve read static noise margin (RSNM). To improve RSNM, a differential 9T SRAM cell [7] was proposed with increase in read operation delay. The low power 10T SRAM cell in[8] provide performance like 9T along with improved leakage due to tail transistor. This paper proposes an optimized high performance 10T SRAM cell (hereafter called OHP10T) and compare the result with differential 6T, 9T and low power 10T SRAM (hereafter called LP10T).

The remaining paper is organized in the following order. Section II presents the Existing and proposed 10T SRAM cell design and device sizing, Section III presents simulation result and its analysis and Section IV presents the concluding remarks.

2. EXISTING AND PROPOSED 10T SRAM CELL

This section presents a novel optimized high performance 10T SRAM cell (OHP10T) as shown in fig. 4 and compared the result with 6T, 9T, LP10T as shown in fig.2, fig.3 and fig.4 respectively. Here, minimum width devices are used to for fair comparison of read SNM, write SNM and feedback pull-up strength. These strict constraints on the device sizing of conventional 6T cell are maintained for fair comparison with the existing and proposed design (cell ratio = pull-up = 1.33).

2.1 Device Dimension of 6T SRAM cell

The size ratio of pull-down device to the access device, referred to as the cell ratio is critical in case of 6T SRAM cell due to its direct read mechanism. The cell ratio determines how high the node QB that stores "0" rises during read access due to voltage dividing effect between driver and access MOSFETs. Typically, cell ratio 1.2–3 is required to avoid read upset in conventional 6T SRAM cell [9]. Write-ability of SRAM cell is determined by the pull-up ratio. Generally, pull-up ratio less than 1.8 is required to maintain good write-ability [10]. Therefore, for maintaining appreciable read stability, write-ability and feed-back pull-up strength minimum width devices are typically not used in standard 6T SRAM cell.

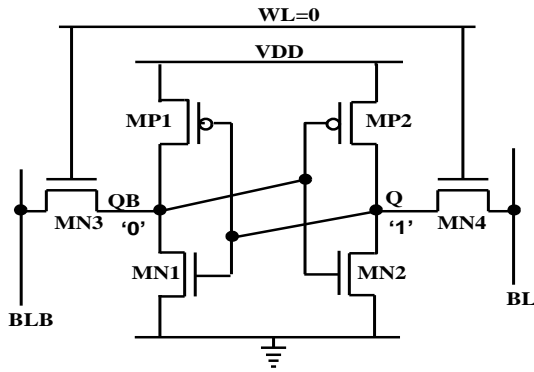


Fig :1 Conventional 6T SRAM cell

2.2 Device Dimension of 9T SRAM cell

This design is based on indirect read and direct write mechanism. The content of 9T cell remains unchanged after each read operation [7]. So, it is called indirect read mechanism. The 6T cell can't offer appreciable read stability. Therefore, this design added extra devices MN5/MN6/MN7 in 6T cell to improve the read stability.

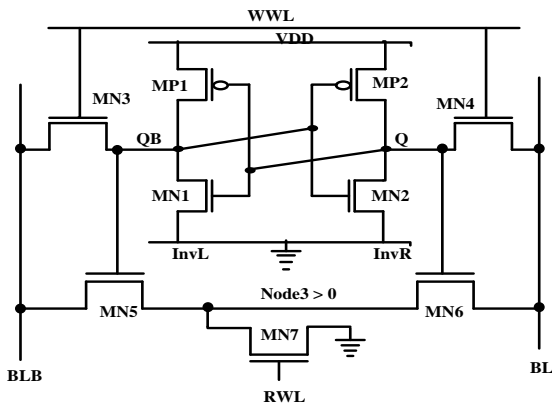


Fig 2: 9T SRAM Cell

2.3 Device Dimension of LP10T SRAM cell

Existing 6T and 9T still suffer with severe leakage. To minimize the leakage power further the tail transistor MN8 is added in stack between pull down transistor and ground. This transistor enables during read and writes [8]. Therefore, in idle mode LP10T operate in sub threshold region.

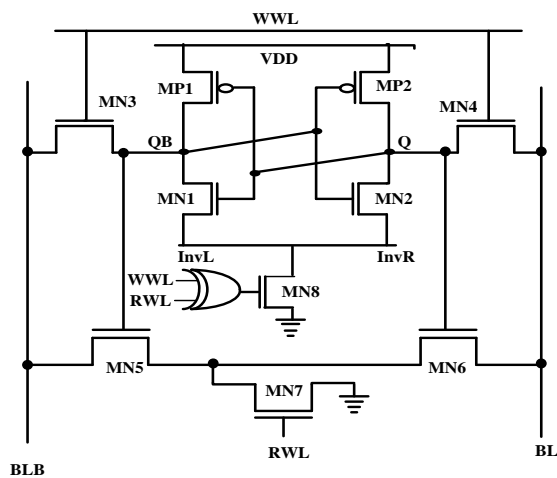


Fig 3: LP10T SRAM Cell

2.4 Device Dimension of OHP10T SRAM cell

This design offer two read driver one for direct read and another for indirect read while only one way of direct write operation. The critical design strategy of our cell is the access transistor MN3/MN4 and tail transistor MN8 are controlled by XOR gate, which is driven by RWL and WWL. The read driver transistors MN6/MN7/MN8 are controlled by RWL as shown in Fig. 4.

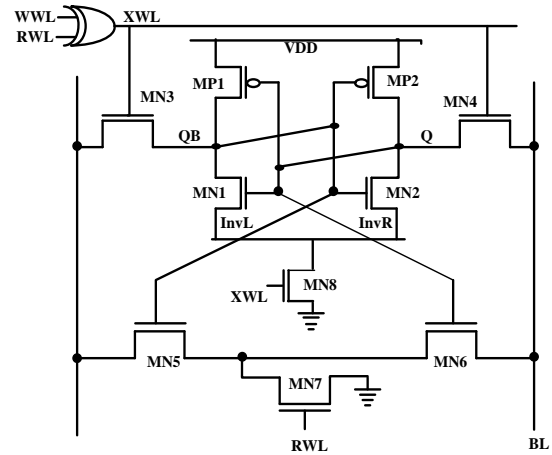


Fig 4: OHP10T SRAM cell

3. SIMULATION RESULT AND ITS ANALYSIS

This section cover the read delay, write delay, read NM , write SNM, standby power and layout area comparison among various existing 6T, 9T, LP10T and Proposed SRAM cell. Complete results are simulated in HSPICE at 22nm technology node [11].

3.1 Read delay

The proposed bit cell exhibits 40% (12%) smaller read delay as compare to LP10T (6T) at nominal V_{DD} prior to read operation. In case of 6T, bit lines are pre charged MN1 is ON, storage node "QB" stores a "0" and "Q" stores a "1"(assumed) when WL(word line) is activated BLB drops through MN3/MN1. Prior to read operation, in proposed OHP10T storage node "QB" store "0" and "Q" store "1" (assumed). Additional indirect read driver performs slower read but offer higher RSNM while direct read driver performs faster read along with smaller RSNM. The combination of both driver offers faster read than existing 6T, 9T and LP10T.

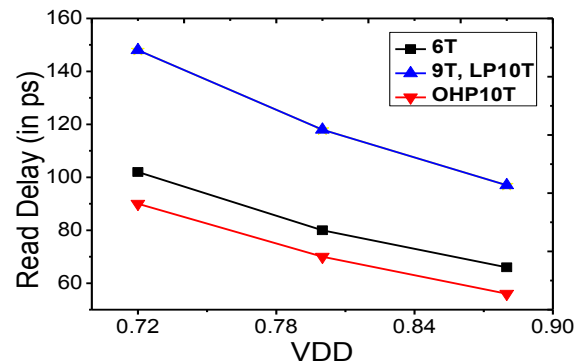


Fig 5: Read delay comparison at different VDD

As shown in Fig.5, Proposed design offers higher read current hence it take smaller time to discharge BL/BLB. The proposed cell offers smaller read delay due to double read driver.

3.2 Read delay

Similar LP10T write, the proposed write delay is estimated as the time required for flipping the state of node that store ‘1’ after activating XOR output XWL. As PU and access devices are mainly responsible for the write delay and they are of same sizes in all the four cells, hence, only marginal 2% penalty in the write delay is observed due to the tail transistor in OHP10T as like LP10T compared with the 6T and the 9T cell shown in Fig.6.

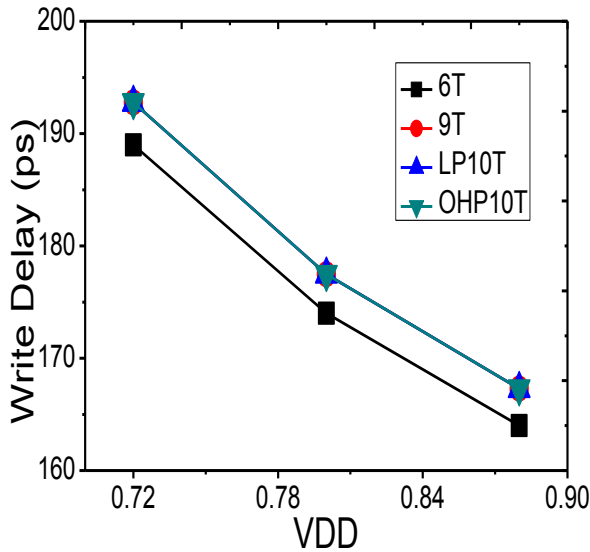


Fig 6: Write delay comparison at different VDD

3.3 Write SNM

The write ability of an SRAM cell is gauged by WSNM (write static noise margin) as shown in fig.4 .The WSNM is a measure of ability of the cell to pull down the node storing ‘1’ to a voltage less than the V_M (switching threshold) of the other inverter storing ‘0’ so that flipping of the cell state occurs. There is a rationed fight between the pull-up PMOS that tries to maintain a ‘1’ and the access NMOS that tries to pull it down [12].

As mentioned, earlier the write-ability of the cell depends on pull up transistor MP1 & MP2 to access transistor MN3 & MN4 strength ratio called pull-up ratio. The write-ability of a cell is estimated using read and write VTCs (voltage transfer curves) [13]. When WSNM falls below zero, write VTC intersects read VTC, indicating positive write margin and signifying write failure[14,15]. As can be seen in Fig. 7, standard OHP10T offers 1.15X higher WSNM as compared with LP12T.

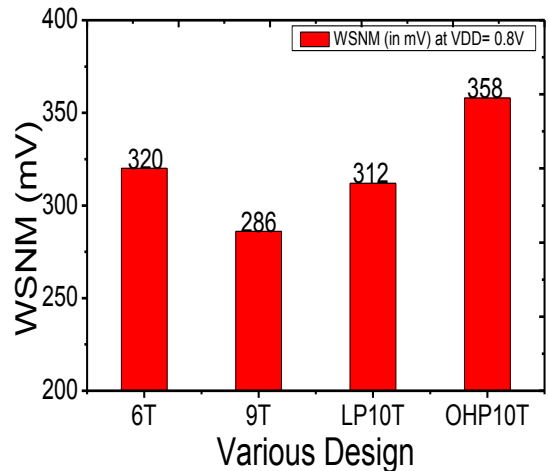


Fig 7: WSNM comparison at different VDD

3.4 Read SNM

The SRAM cell is most vulnerable to noise during read operation since the node storing ‘0’ rises to a voltage higher than ground due to the voltage dividing effect between the access transistor and inverter pull down NMOS driver. The size ratio of pull down transistor to the access transistor, referred to as the cell ratio, determines how high the ‘0’ storing node rises during read access. The smaller cell ratio translates into higher voltage drop across the pull down transistor, requiring a smaller noise voltage at the node storing ‘0’ to trip the cell [16]. Therefore, RSNM is more critical design metric of SRAM cell than Write SNM. Fig.7 show that OHP10T offers 48% higher RSNM as compared with 6T.

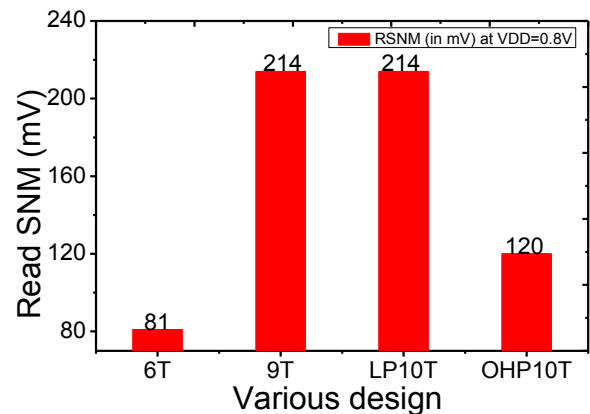


Fig 8: WSNM comparison at different VDD

3.5 Standby Leakage Power

The standby leakage in embedded cache is an alarming issue in deep-submicrometer technology since several ten of million identical cells are common in today’s caches. The leakage current is one of the major contributors to the total power dissipation in an embedded SRAM cell because a major part of the cache remains idle most of the time except for the row being accessed. The total leakage current in an SRAM cell mainly (neglecting other minor leakage components such as GIDL leakage and punch through leakage) consists of the subthreshold leakage current (I_{sub}), the gate leakage current (I_g), and Junction leakage current (I_{JN}) through different devices.

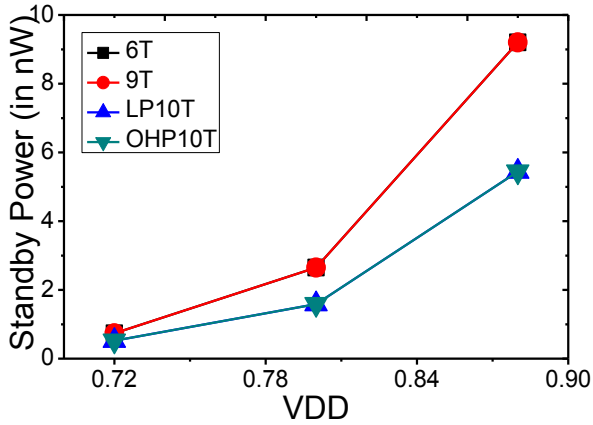


Fig 9: Standby leakage power comparison at different VDD

As subthreshold leakage in hold mode is the major leakage component that is reduced due to tail transistor[17,18]. The proposed design dissipates 40% smaller leakage power compared with 6T and 9T while similar as LP10T(see Fig10). As observed, the proposed bitcell reduces leakage power at all considered V_{DD} . The comparison of leakage power at different V_{DD} is shown in Fig.9.

3.6 Comparison of leakage power versus temperature

Since VLSI circuits often operate at elevated temperature, we have simulated the cell varying temperature in the range from 25°C to 150°C for estimation of leakage power, because leakage power becomes incremental at higher temperature as shown in fig.10. This is because the I_{sub} (threshold current) controlled by the carrier diffusion, increase exponentially with temperature.

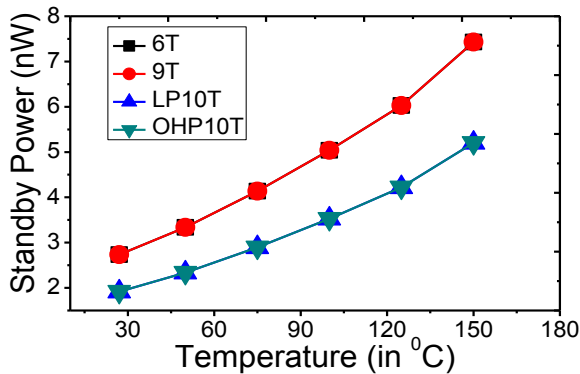


Fig 10: Standby leakage power comparison at different temperature

3.7 Layout Area

Due to lack of unavailability of 22-nm layout tool for a precise layout area comparison of 6T, 9T, LP10T and OHP12T, layouts are generated using 45-nm design rules. The area of the generated proposed bit cell OHP10T (shown in Fig.13) is found to be $54 \lambda \times 32 \lambda$ (column height \times column pitch) against 6T $53 \lambda \times 24 \lambda$. Thus, our bitcell occupies 38% area overhead compared to 6T SRAM cell. The estimated area overhead is 5% if the area occupied by XOR gate is shared among the cells of the single row. If the word size is increased, the area overhead per cell will be reduced as the XOR gate need not be

upsized[19]. Thus, the area occupied by OHP10T is similar as LP10T and 38% larger than 6T.

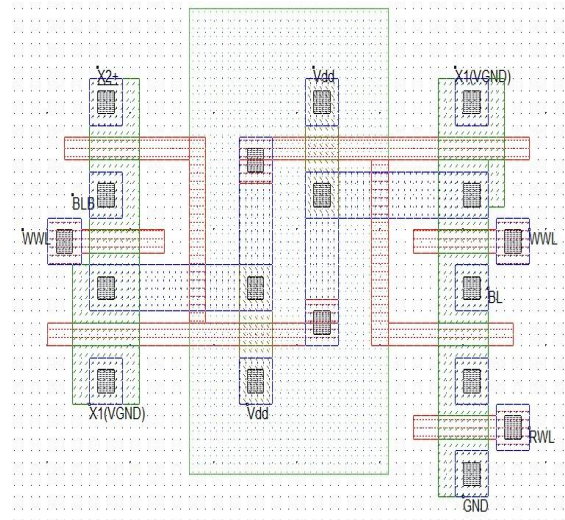


Fig 11: Layout diagram of OHP10T

4. CONCLUSION

This work proposes an optimized high performance 10T SRAM cell. It analyzes the impact of PVT improvement in the most of the design parameters over standard 6T, 9T and LP10T SRAM cell demonstrating its reliability, smaller read delay and moderate RSNM. This design occupies similar layout area like LP10T instead of appreciable improvement on read access time as compared with 6T, 9T and LP10T. This cell obtain 40% smaller read delay and 15% higher WSNM as compared with LP10T.

5. ACKNOWLEDGMENTS

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