A New Approach of Presenting Universal Reversible Gate in Nanoscale

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ABSTRACT
Quantum dot Cellular Automata (QCA) is an emerging digital logic representation techniques and one of the possible alternatives to Complementary Metal–Oxide–Semiconductor (CMOS) technology. It satisfies attractive circuit components of smaller size and low power dissipation of new circuit design technologies. Quantum dots are nano architecture and it works based on columbic interaction between two electrons. This paper presents Universal Reversible Gate based on QCA logic gates. For simulating and verifying the proposed gate QCA Designer a familiar simulation and verification tools has been employed. Correctness of the proposed circuit revealed by the simulated output. This paper also presents the VHDL Code of this circuit.

General Terms
Quantum Cellular Automata, Reversible Logic Gates and VHSIC Hardware Description Language.

Keywords
Quantum dot Cellular Automata (QCA), QCA logic gates, Universal Reversible logic Gate (URG) in QCA, Majority Voter (MV) gate.

1. INTRODUCTION
Quantum-dot cellular automata are promising and efficient technologies to replace CMOS technology. QCA have attracted a lot of attention for its extremely small feature size and ultra-low power consumption [1, 2]. Cell is the fundamental element of QCA and it consists of two quantum dots and two mobile electrons[3, 4]. The electrons are impulse to the corner positions due to coulombic repulsion [5]. Depending on the electron's position, QCA cell has two form of polarization, P = -1 or binary 0 and P = +1 or binary 1 [2] shown in figure 1. The equation for the cell polarization [2] is given below:

$$P=\frac{(\rho_2+\rho_4)-(\rho_1+\rho_3)}{(\rho_1+\rho_2+\rho_3+\rho_4)} \quad (1)$$

Where, the electronic charge at dot *i* denoted by ρ_i

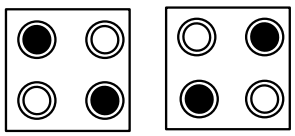


Fig 1: Illustration of four doted QCA cell with binary encoding representation

QCA wire is a collection of interconnected QCA cells with the same polarization which is used to transmit signal one place to another place. Two different form of QCA are constructed to transfer data in QCA. One is binary QCA wire constructed by 90°cells and the other is the inverter series of QCA cells which is constructed by 45°cells. Figure 2 illustrates the structure of two wire types.

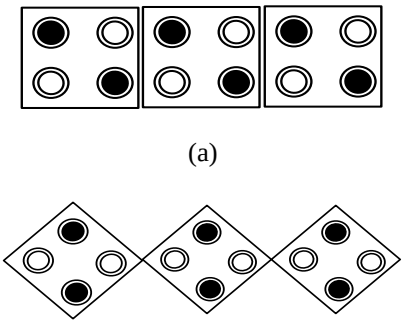


Fig 2: QCA Wire (a) 90^o(b) 45^o

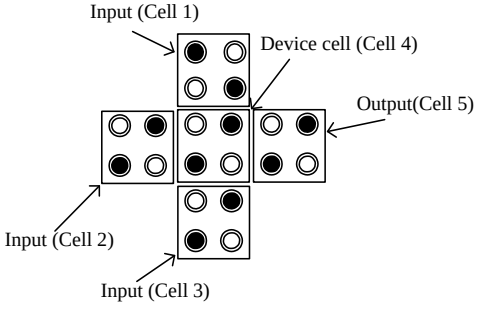
Three input majority gate (Maj3) is the primitive logic gate in QCA.Maj3can be comprehend by five cells, three inputs, one output and unique middle cell. The middle cell also known as device cell which switches to main polarization and resolves the durable output. Maj3 can be operated as a 2-input AND or a 2-input OR logic gate, simply by fixing one of the three input cells polarization to p = -1 or p = +1, respectively shown in figure 3. The logical expression of Maj3 is as follows:

$$\mathbf{MV(A,B,C) = AB + BC + CA} \quad (2)$$

To make "AND" and "OR" gate, we need to set one of the MV input fixed to zero or one. Equation (3) presents the AND gate operation when C=0 and Equation (4) presents the OR gate operation when C=1.

$$\mathbf{MV(A,B,0) = AB + A.0 + B.0 = AB} \quad (3)$$

$$\mathbf{MV(A,B,1) = AB + A.1 + B.1 = A + B} \quad \mathbf{(4)}$$



(a)

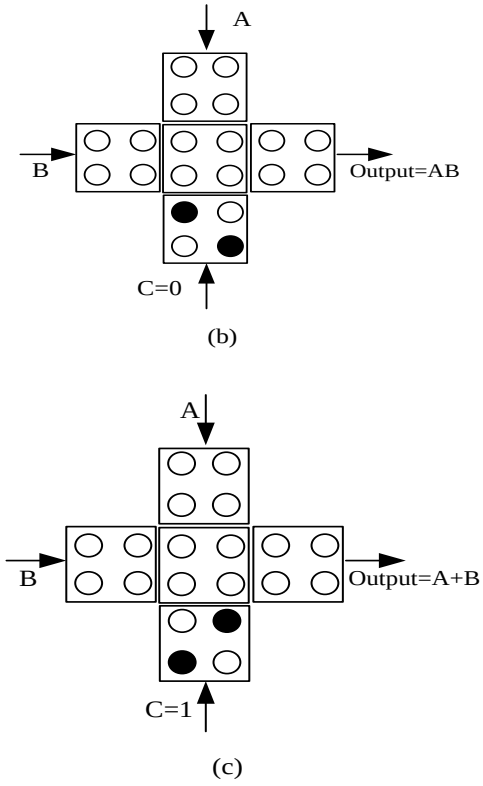


Fig 3: Basic structure of 3-input majority voter gate (a), programmed as 2-input AND gate (b)and 2-input OR gate (c)

2. METHODLOGY

The proposed circuit was functionally simulated using the QCA Designer [16].Analysis is implemented to find out the required tools and to verify the proposed circuit. The proposed circuit layout is simulated and tested using QCA Designer 2.0.3. The bistable simulation engine has been employed during the simulation interaction between cells, explicitly the communication strength involving two cells decomposes contrarily with the fifth power of the width unraveling them. In this approximation not all the cells effect are pondered. Only cell within the radius of R are being considered. For cell i, the mathematically model is described by the following Hamiltonian:

$$\mathbf{H_i} = \sum_j \begin{pmatrix} -\frac{1}{2}\mathbf{P_j}\mathbf{E}^{\mathbf{k}}_{\mathbf{i,j}} & -\boldsymbol{\gamma} \\ -\boldsymbol{\gamma} & \frac{1}{2}\mathbf{P_j}\mathbf{E}^{\mathbf{k}}_{\mathbf{i,j}} \end{pmatrix} \quad (5)$$

Eki,j is the kink energy between the two cells (I and j); Pj represents the polarization for cell j and tunneling energy is ϒ. For each cell i, the sum of the Hamiltonian is over all cells (i.e., j) within its radius of effect R.

3. PROPOSED CIRCUIT AND PRESENTATION

Reversible computing is a computational paradigm in which the number of inputs and number of outputs are identical with one-to-one mapping. Reversible logic has received immense attention due to their capacity to diminish the power dissipation. The most impressive function of reversible logic lies in quantum computing [6] and it can be implemented through quantum dot cellular automata [7, 8, 9, 10, 11, 12, 13, 14,15]. This paper presents the design formation of a reversible "URG" logic gate.

3.1 Universal Reversible Gate

Universal Reversible Gate (URG)is a 3x3 gate with input vector I(A, B, C) and output vector O(P, Q, R).The outputs are P= (A+B)⊕C, Q=B, R= AB⊕C. Figure 4 shows the QCA circuit diagram of 3x3 Universal Reversible gate and table 1 shows the truth table of this gate.

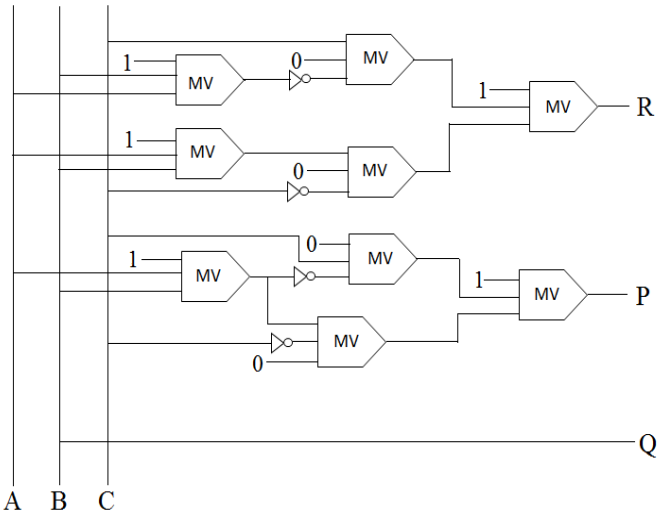


Fig 4: Circuit diagram of URG

Table 1. Truth table of URG

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	1
1	1	1	0	0	1

3.2 VHDL design

VHDL is generally used to write text models which depict a logic circuit. Combinational circuit of all elemental reversible logic gates can be demonstrated through simulations using VHDL. Figure 5 shows the combinational circuit diagram of3x3 URG.

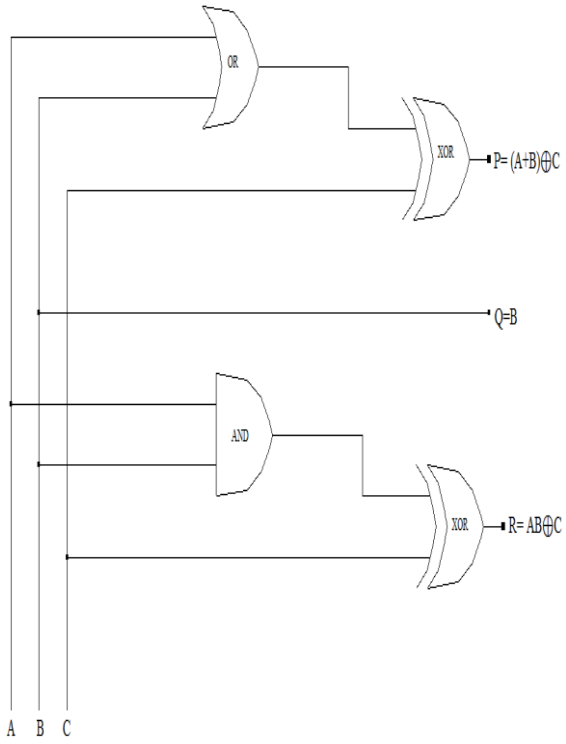


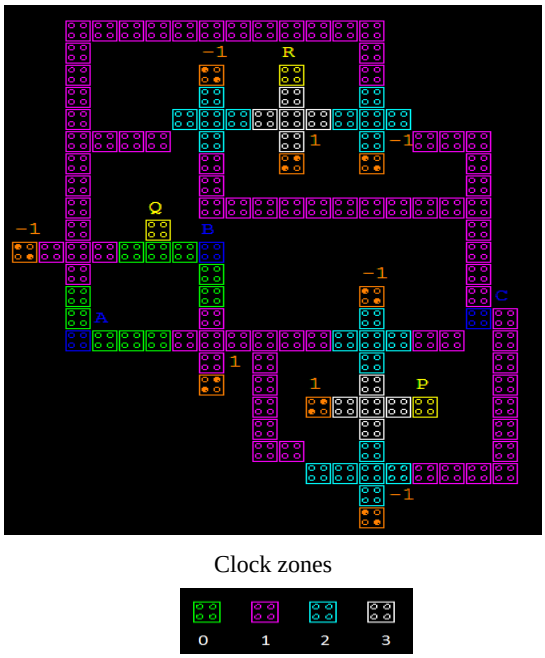
Fig 5: Combinational circuit diagram of 3x3 URG

The VHDL for 3x3 URG is shown below:

```
library IEEE;
use IEEE STD_LOGIC.1164.ALL;
entity urg is
    Port(A, B, C : in STD_LOGIC;
         P, Q, R : out STD_LOGIC);
end urg;
architecture Ckt of  urg is
signal S1, S2 : STD_LOGIC;
begin
S1<=A or B;
P<=S1 xor C;
Q<= B;
S2<= A and B;
R<= S2 xor C;
end Ckt;
```

4. SIMULATION AND RESULT

Our proposed circuit has been designed and simulated using the QCA Designer [16] a familiar simulation tool for QCA device. Bistable approximation has been applied with below default parameters: cell size= 18nm, number of samples= 50000, convergence tolerance= 0.0000100, radius of effect= 65.000000nm, relative permittivity= 12.900000, clock high= 9.800000e–022 J, clock low= 3.800000e–023J, clock amplitude factor= 2.000000, layer separation= 11.500000 and maximum iterations per sample= 100.These are the fixed parameters in QCA Designer. In the circuit design two fixed polarization P= 1.00 and P= -1.00 is used. These two polarizations are used to change the logic state. The circuit layout of our proposed gate is shown in figure 5 and the simulated waveform is shown in figure 6.



Clock zones

Fig 6: Simulated circuit layout of URG in QCA

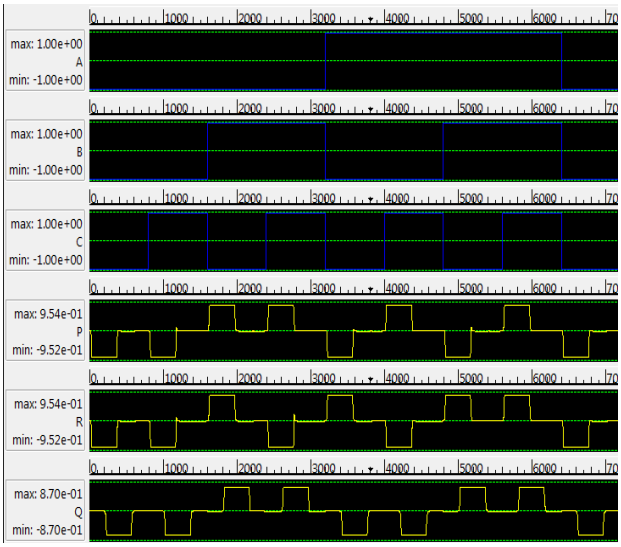


Fig 7: Simulated waveforms for URG

Table2.Performancecriterion of proposed gate

Parameter	URG
Number of cells	134
Time delay(clock cycle)	1
Number of clock	4
Area(μm^2)	0.173

5. CONCLUSION

This paper explores an efficient approach of Universal Reversible Gate (URG) based on QCA technology. Practical use of URG in the improvement of combinational circuits would be gainful in respect of power saving and delay. The

proposed gate is helpful for future computing like ultra-low power advanced circuits and quantum computing. VHDL is best suited to the design and specification of digital electronic hardware. The simulation outcome confirmed that the proposed circuit executes well. Hence, it concludes that the proposed layout should be promising step towards the intention of low power design in nanotechnology.

Forthcoming work can be extended as to design systems to handle extensive circuits along the inevitable goal of synthesizing quantum circuits.

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