Comparison of Leakage Power Reduction Techniques in 65nm Technologies

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ABSTRACT
The rapid progress in semiconductor technology have led the feature sizes of transistor to be shrunk there by evolution of Deep Sub-Micron (DSM) technology; there by the extremely complex functionality is enabled to be integrated on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. Leakage power consumption is one of the major technical problem in DSM in CMOS circuit design. A comprehensive study and analysis of various leakage power minimization techniques have been presented in this paper comparison of Leakage reduction technique is developed in Cadence Virtuoso in 65nm regime with the combination of stack with sleepy keeper approach with Low V_{th} & High V_{th} which reduces the Average Power with respect Basic Nand Gate 29.43%, 39.88%, Force Stack 56.98, 63.01%, sleep transistor with Low Vth & High Vth 13.90, 26.61% & 33.03%, 75.24% with respect to sleepy Keeper 93.70, 56.01% of Average Power is saved.

Keywords
Leakage Reduction, High speed, Low power, DSM

1. INTRODUCTION
Leakage power consumption is an important issue in DSM CMOS VLSI circuit. The main contribution of Power dissipation in CMOS circuit increases with the reduction of channel length, threshold voltage and gate oxide thickness.

The power dissipation of a logic gate is given by:-

Pavg /gate = Pswitching + Pshort circuit +Pleakage 1.1

Where Pswitching is the power dissipated due to charging and discharging of the circuit capacitances, Pshort circuit is the power dissipated due to the short circuit between Vdd and ground during output transitions and P leakage is the power dissipated due to leakage current. The term, Pleakage, is dramatically increased with technology down scaling and increase in temperature, resulting in a reduction of leakage [2] immunity and robustness. Therefore, it is very vital to reduce the leakage power of dynamic logic gates. High leakage current in nanometer regime becomes a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. Leakage power depends on gate length and oxide thickness and it varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors helps to reduce dynamic power dissipation but simultaneously leakage power increases

The organization of the paper is as follows: The section II, describes previous work which consist various types of leakage current and techniques to reduce the leakage current. Section III presents simulation result using Cadence EDA. Finally the conclusion is presented in section IV.

2. PREVIOUS WORK
There are various types of Leakage current present in CMOS devices as we scale down the channel length some of the Leakage current present in CMOS are[5]

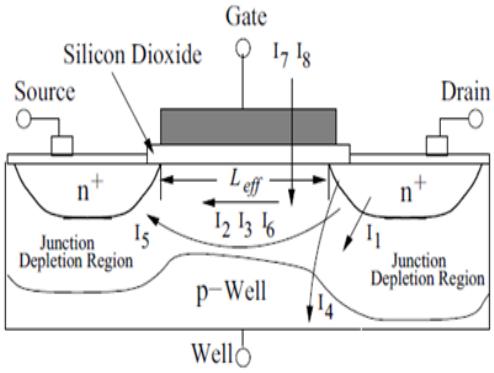

Fig.1. Leakage Mechanism in Short-Channel NMOS Transistor

I1= Reverse-bias p-n junction diode leakage current

I2 = Subthreshold leakage current

I3 = Gate Oxide tunneling current

I4 = Hot-carrier injection

I5 = Channel punch-through

I6 =Gate induced drain-leakage current

2.1 Leakage Power Reduction Technique
A. Sleep Mode Approach
For reduction of subthreshold leakage current in DSM is the sleep approach[6]. In sleep approach we insert a additional transistor in header & footer of the basic circuit. The sleep transistor PMOS is inserted between Pull up network and V_{dd}. NMOS transistor is inserted between pull down network of the circuit and GND[2]. These sleep transistors turn off the circuit by cutting off the power rails. Fig.1. shows the structure of sleep approach. The sleep transistors are turned on when the circuit is active and provide very low resistance in

the conduction path so that circuit"s performance will not affects due to these additional transistors [3]. During the standby mode these transistors are turned off and introduce large resistance in the conduction path so that leakage power is reduced in the circuit. By rail out from the V_{dd} we can reduce leakage power effectively [2,9].

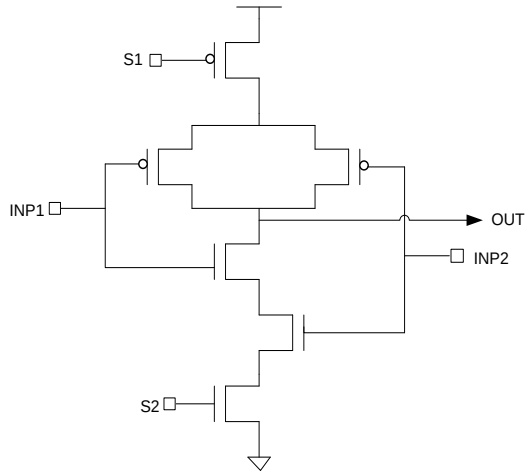

Fig.2. Sleep Approach NAND gate

B. Stack Approach

Another leakage power reduction technique is, which forces a stack affect by dividing existing transistor into two half size transistors and maintain the W/L ratio of the transistor. The threshold voltage variation results in increase Sub-threshold leakage, and the threshold voltage changes due to body effect [4]. From these two facts, one can reduce the subthreshold leakage in the device by stacking two or more transistors serially [5]. The transistors above the lowest transistor will experience a higher threshold voltage due to the difference in the voltage between the source and body as shown in Fig.3. Also, the V_{ds} of the higher transistor is decreased, since the intermediate node has a voltage above the ground. These results in reduction of DIBL effect hence better leakage savings. However, forced stack devices have a strong performance degradation that must be taken into account when applying the technique [3-5].

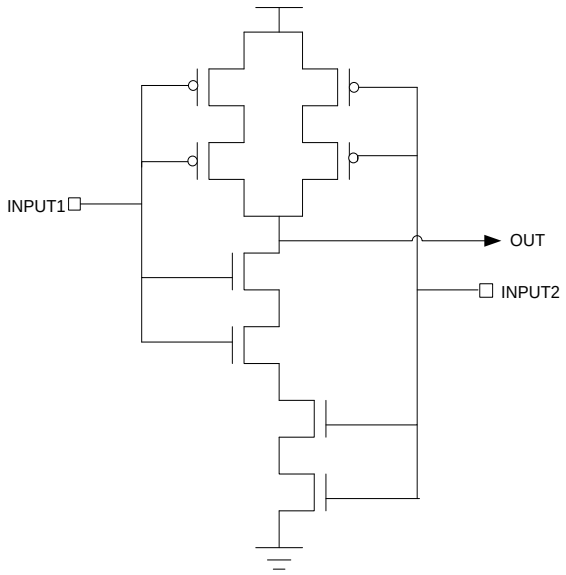

Fig.3. Stack Approach based 2 input NAND gate

C. Leakage Feedback Approach

Leakage feedback approach uses two additional transistors to maintain logic state during sleep mode, and the output of the inverter is derived by the two transistors output of the circuit implemented utilizing leakage feedback [5-6].

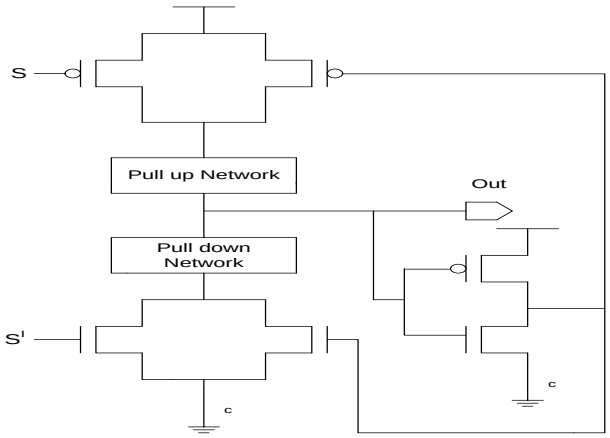

Fig.4. Leakage Feedback Approach

As shown in Fig.4. a PMOS transistor is placed in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S'). The two transistors are driven by the output of the inverter which is driven by the output of the circuit. During sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail.

D. Sleepy Stack Approach

The main idea behind the sleepy stack technique is to combine the sleep transistor approach during active mode with the stack approach during sleep mode. The structure of the sleepy stack approach is shown in Fig.5. The sleepy stack technique divides existing transistors into two transistors each typically with the same width half the size of the original single transistor"s width. Then sleep transistors are added in parallel to one of the transistors in each set of two stacked transistors; the divided transistors reduce leakage power using the stack effect while retaining state [5]. The sleepy stack technique divides existing transistors into two transistors each typically with the same width W1 half the size of the original single transistor"s width (i.e.W1 = W0/2), thus, maintaining equivalent input capacitance. The added sleep transistors operate similar to the sleep transistors used in the sleep technique in which sleep transistors are turned on during active mode and turned off during sleep mode [6]. During active mode, S=0 and S'=1 are asserted, and thus all sleep transistors are turned on. Due to the added sleep transistor, the resistance through the activated (i.e., "on") path decreases, and the propagation delay decreases (compared to not adding sleep transistors while leaving the rest of the circuitry the same, i.e., with stacked transistors). During the sleep mode, S=1 and S'=0 are asserted, and so both of the sleep transistors are turned off. The stacked transistors in the sleepy stack approach suppress leakage current. Although the sleep transistors are turned off, the sleepy stack structure maintains exact logic state. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high- transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. By combining these two effects, the sleepy stack structure

achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. The price for this, however, is increased area [4].

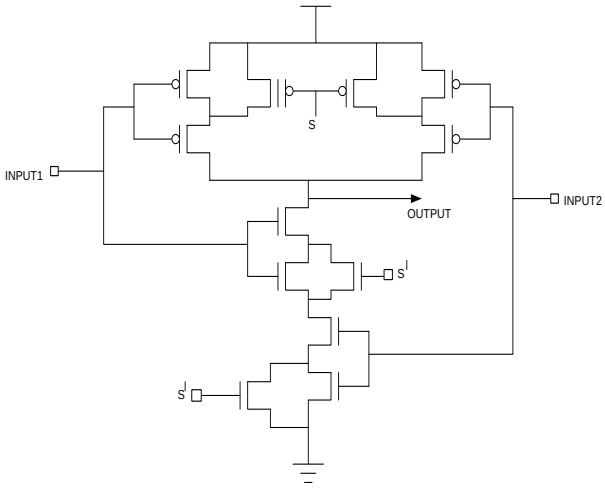

Fig.5. Sleepy Stack Approach based 2 input NAND gate

E. Sleepy Keeper Approach

The most efficient approach for leakage power reduction is sleepy keeper approach. As we know that PMOS transistor is connected to Vdd & NMOS transistor is connected to GND . A NMOS transistor will not pass Vdd efficiently, so to overcome this problem to maintain a value of "1" in sleep mode, the sleepy keeper approach is used. The sleepy Keeper approach maintain output value of "1" and connect NMOS transistor to Vdd to maintain output value equal to "1"in sleep mode as shown in Fig.5.[5]. An additional NMOS transistors place parallel to the sleep transistor of pull up network to connect Vdd in sleep mode when PMOS is rail off [9].Similar case will repeat in pull down network a PMOS transistor is inserted parallel to the pull down sleep transistor to maintain output value equql to "0" when in sleep mode. For sleepy stack approach we need to connect NMOS to Vdd and PMOS to GND to maintain the proper Logic [7-8].

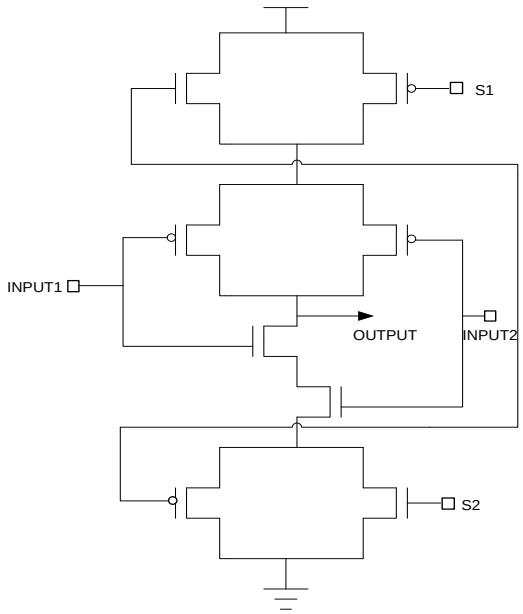

Fig.6. Sleepy keeper Approach based 2 input NAND gate

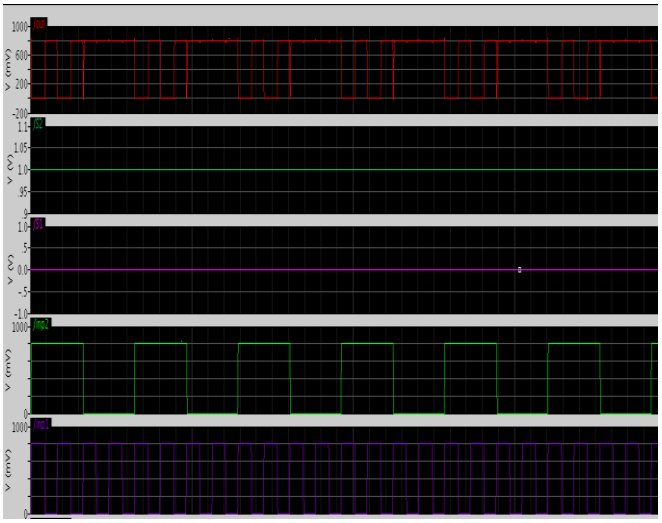

Fig.7. Output waveform of Sleepy Keeper approach with 2 input NAND gate.

F. RBB Scaling with Technology

Among the leakage power reduction techniques, the reverse body biasing (RBB) technique, which increases the threshold voltage Vth of transistors during standby mode, has widely been employed to suppress the subthreshold leakage current (Isub) [11,12]. Body bias is dynamically adjusted to forward body bias in active mode to increase performance and reverse body bias in standby mode to reduce leakage [13]. As we are reducing the static power consumption of the circuit we have applied only the reverse body bias. Since the subthreshold leakage current (Isub) is the major leakage component, the RBB technique is used to reduce the total leakage current in standby-mode CMOS circuits by increasing the transistor threshold voltage. However, it is important to watch how other leakage current components change when the RBB is used to estimate the total leakage. By applying to a transistor we can further increase the threshold voltage of the transistor. In our work we are showing the effect of RBB on the static power consumption of the NAND gate. In existing technique are using RBB on the existing leakage reduction techniques. However applying RBB to pull down network comes with delay problems as RBB decreases the switching speed of the circuit

Table 1. Threshold voltage of NMOS and PMOS

Threshold	Transistor voltage
NMOS Low V_{th}	-37mV
NMOS high V_{th}	345mV
PMOS low V_{th}	-83mV
PMOS high V_{th}	-393.9mV

3. COMPARATIVE ANALYSIS OF SIMULATION RESULTS

A 2 input NAND gate is simulated with leakage power reduction techniques sleep, forced stack, sleepy keeper and sleepy stack with DTCMOS. After analyzing the results in terms of average power consumption, delay and PDP we conclude that sleepy stack with DTCMOS is producing comparatively better results. Simulations are done on Cadence Vertuso simulator at 65nm technology and supply voltage of

0.8V. The circuits are simulated with high threshold and low threshold NMOS and PMOS transistors.

These circuit's schematics are designed on cadence virtuoso schematic editor and simulated it by using spectre simulator on cadence virtuoso specter version 5.1.0. 65nm process technology has been used for designing these circuits. Table III. Shows the the results obtained for 2 input NAND gate with dual threshold transistors and reverse body bias and without reverse body bias in dynamic power calculation. The simulation results for 2 input NAND gate with sleep, forced stack, sleepy keeper and sleepy stack with DTCMOS and RBB are shown in the following table IV. in static power calculation for reduction of leakage power in nanosacle circuit design

Table.2. Average power, Dynamic power, Static power, Delay and PDP for 2 input NAND gate

65nm	Dynamic power (nW)	Static power (pW)	Delay (pSec)	PDP (1E-21)	EDP (1E-33)
Base	47.15	197.4	18.212	3.595	65.47
Sleep	48.91	54.74	16.9	.925	15.63
Forced stack	68.65	67	19.23	1.288	24.76
Sleepy keeper	48.47	118.5	19.26	2.278	43.87
Sleepy stack	63.24	58.06	21.268	.791	16.82

Table 3. Percentage dynamic power saving for each Technique with RBB

65nm	Dynamic power(nW) With RBB	Dynamic power(nW) without RBB	Percentage saving (%)
Sleep	42.97	48.97	13.96
Forced stack	61.62	68.72	11.52
Sleepy keeper	42.79	48.59	13.55
Sleepy stack	63.24	50.57	19.90

Table 4. Percentage static power saving for each technique with RBB

65nm	Static power(nW) with RBB	Static power(nW) without RBB	Percentage saving (%)
Sleep	24.04	54.74	127.70
Forced stack	15.45	67	333.65
Sleepy keeper	35.97	118.5	229.44
Sleepy stack	17.7	58.06	228.02

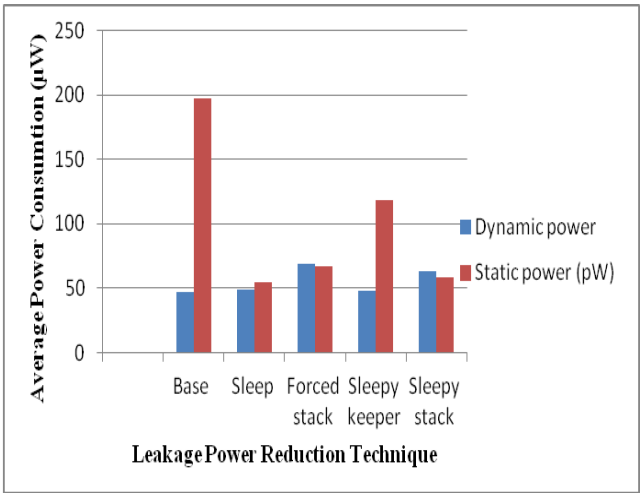

Fig.8. Comparison of Average Power consumption of sleep, forced stack, sleepy keeper and sleepy stack

4. CONCLUSION

In nanometer scale CMOS technology, subthreshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. RBB has a combined structure of four well-known low-leakage techniques, which are the forced stack, sleep transistor techniques, RBB. However, unlike the forced stack technique, the sleepy stack technique can utilize high-Vth transistors without incurring large delay overhead however, unlike the forced stack technique; the sleepy stack technique can utilize high-Vth transistors without incurring large delay overhead. Also, unlike the sleep transistor technique, the sleepy stack technique can retain exact logic state while achieving similar leakage power savings. In short, our sleepy stack structure achieves ultra-low leakage power consumption while retaining state.

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