The Design and Optimization of MOSFET Driving Circuit based on Parasitic Parameter

Wei Hong
Shanghai University of Engineering Science
Songjiang Shanghai
201620, China

Yuchen Chen*
Shanghai University of Engineering Science
Songjiang Shanghai
201620, China

Zhengming Li
Shanghai University of Engineering Science
Songjiang Shanghai
201620, China

ABSTRACT
According to the parasitic parameter which was produced by the PCB line of MOSFET's driving circuit, this paper will analyze the circuit principle of driving circuit, and then uses the software Saber to stimulate the circuit, finally verifies the stimulate results and formula under the experimental waveforms and statics.

General Terms
Stimulation and Hardware Design

Keywords
Saber stimulation; Miller effect; driving circuit; parasitic parameter; MOSFET

1. INTRODUCTION
With the development of power electronics technology the Switching power supply technology has matured, its high conversion efficiency and high level of stability and reliability make it gradually replaced the traditional linear power supply. People usually pursue high power density and high efficiency switching power supply. Usually there are two methods to increase power density and efficiency: one is to reduce the loss of switch topologies, which reduces the volume of heat sink; the other is the means to realize high frequency switch power supply, so as to reduce the volume of passive components.

In practical applications, to the aim of easing the design, people usually use the way to increase the frequency of switching. In the switching power PCB's production, the drive circuit will inevitably produce parasitic parameters. When it is at a low switching speed , these parasitic parameters may have little effect, but once in the high-speed PCB design, parasitic parameters of circuit will cause some strange effect, it will not only reduce the electromagnetic compatibility EMC, but also greatly increase the switching losses. Particularly is the driving circuits and MOSFET structure alignment, these factors will affect reliable capability of switching, and affect the overall stability of switching power-supply system.

2. DESIGN AND ANALYSIS OF DRIVING CIRCUIT

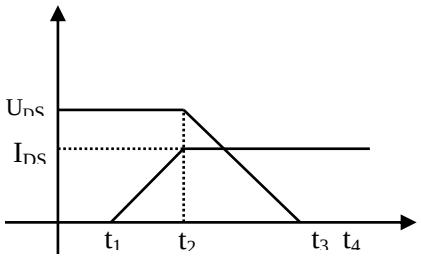

Fig 1: The drain-source voltage and current waveform when MOSFET turns on

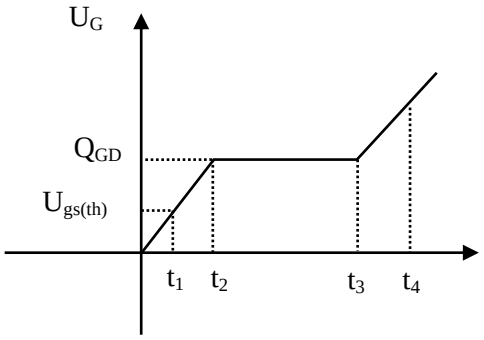

Fig 2: The gate-source voltage waveform when MOSFET turns on

Stage 1(0-t_1): MOSFET accept the drive signals, rise from zero to $U_{GS\ (th)}$, when at t_1 point I_d, I_d at t_1 point is 0.

Stage 2(t_1-t_2): T_1 gate and the source reaches the threshold voltage $U_{GS\ (th)}$, I_d started to increase, I_d reached the maximum value. This time is called the current rise time.

Stage 3(t_3-t_4): Miller platform (t_2-t_3).At the T_2 moment, between the source and drain voltages U_{DS} began to decline, MOSFET can be considered turning on gradually, the drive circuit of the MOSFET' must charge the capacitance between drain, leading to the Miller effect

Stage 4(t_3-t_4), Gate-source voltage increases until it reaches a pre-designed drive voltage., in order to let the MOSFET turn-on reliably, the driving voltage is usually designed about 10V-15V. MOSFET's switching speed is very fast, the MOSFET's driving circuit needs instantaneous peak current, makes Miller platform delay time (t_2-t_3) as short as possible.

The source of the driving circuit is TMS320F2812 DSP chip, The design of driving circuit is based on the optical coupling isolation.

Because TMS320F2812 DSP chip can approximately output about 4mA current, and the current of optical coupling isolation is about 20mA for the chip HCNW2201, so add the Darlington integrated chip ULN2003. "Double-GND" principle can achieve the goal of signal isolation, and it can effectively suppress high frequency clutter signal interference.

In order to make reliable MOSFET switch, this design uses the TC4420 driver chip, it contains two transistors, which can output a pulse whose peak current is 6A, it can meet the needs of the MOSFET's drive.

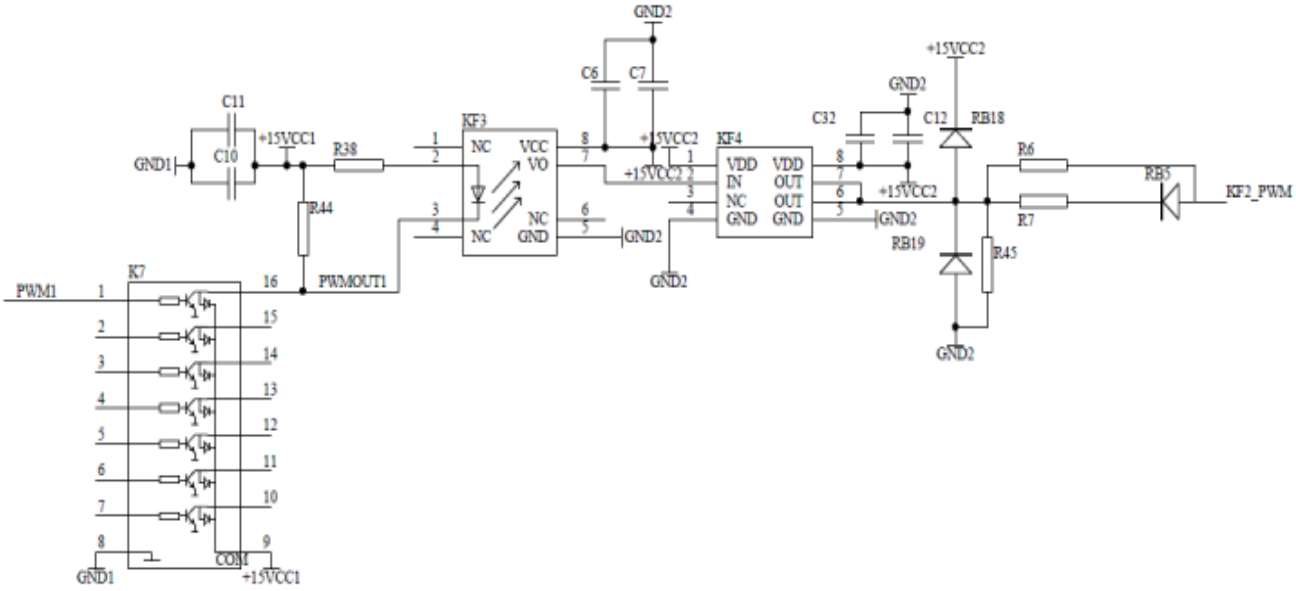

Fig 3: Isolating driver circuit schematic diagram

When people study the effects of parasitic parameters of driving circuit, people mainly consider two aspects: the one is parasitic resistance and parasitic inductance in the packaging structure of the MOSFET; the other is parasitic parameters which caused by the PCB wiring line.

When considered the PCB wiring line, the parasitic inductance is the main factor, self-inductance and mutual inductance can be obtained through empirical formula, the self-inductance L1:

$$L_1 = \frac{\mu_0}{2\pi}\left[ln\frac{2C}{K+H} + 0.5 + \frac{0.2235(K+H)}{C}\right]$$

The unit is (H), u_0 is the permeability of vacuum.

When the PCB line is double parallel line, which will cause mutual inductance, the L_2 by the following formula: the length is c, distance is j, and the mutual inductance calculation formula is as follows [2]:

$$L_2 = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{C}{J} + \sqrt{1+\left(\frac{C}{J}\right)^2}\right) - \sqrt{1+\left(\frac{J}{C}\right)^2} + \frac{J}{C}\right]$$

Usually in practical application, in order to calculate PCB cable inductance simplely, often use the formula:

$$L_3 = L\text{ength} + 10$$

The unit is (nH).

Length: PCB-driven resistance R_g to the MOSFET, the unit is (mm).

When the driver circuit turned on, circuit schematic can be turned into the following figure:

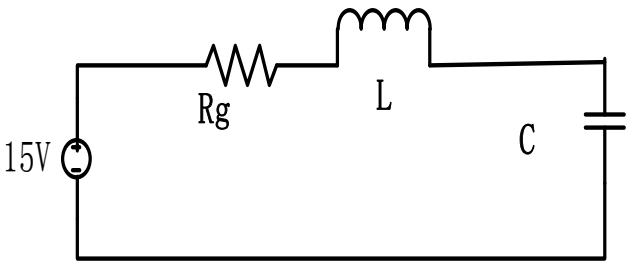

Fig 4: The model of driving circuit when it turns on

L is the parasitic inductance, C is the capacitance between GS and R_g is the driving resistance such as R_6. According to the figure on the circuit, the current of drive circuit:

$$I_g = C\left(\frac{\partial V_C(t)}{\partial t}\right)$$

Inductor's voltage:

$$V_L = L\left(\frac{\partial I}{\partial t}\right)$$

Resistor's voltage:

$$V_g = R_g \times I_g$$

According to the KVL:

$$LC\left(\frac{\partial^2 V_C(t)}{\partial t^2}\right) + C\left(\frac{\partial V_C(t)}{\partial t}\right)R_g + V_C(t) - V = 0$$

The formula can be explained:

$$G = \frac{V}{LCS\left(S^2 + \frac{1}{LC} + \frac{R_g S}{L}\right)}$$

This is a 3-step system, according to its zeros and Poles, several conclusions can be got:

(1) When the poles for 3 different real roots, it will produce over damping vibration;

(2) When the pole has two real roots, it will produce critical damping vibration;

(3) When there are some imaginary numbers, it will produce less damping shocks.

When it causes damping shocks, the MOSFET's gate source drive voltage waveform will produce shock, it will appear a short rise of pointed peak voltage, it can make switch tube failure, so you should bring it to a damping or critical state.

And:

$$V_C(S) = \frac{V_g}{\left(LCS^2 + R_g CS + 1\right)}$$

1.$R_g < 2\frac{\sqrt{LC}}{C}$, the circuit is underdamped, circuit will shock;

2.$R_g = 2\frac{\sqrt{LC}}{C}$, the circuit is in the critical damping States;

3.$R_g > 2\frac{\sqrt{LC}}{C}$, the circuit is in a damp State, the circuit can work well.

To make the driving circuit shock does not occur, the circuit must be in a damping condition, so get the drive resistor:

$$R_g > 2\frac{\sqrt{LC}}{C}$$

And a MOSFET is turned on at the Miller platform stage, rising response time can be calculated:

$$\tau = R_g \times (Ciss - Crss)$$

R_g is the driving resistance, Ciss is MOSFET's input capacitance, Crss is MOSFET's reverse transfer capacitance.

Generally, with the combination of parasitic parameters in a practical application, time constant is calculated by the formula:

$$\tau' = 2 \times R_g \times (Ciss - Crss)$$

Capacitance charging time is less than or equal τ', in order that to make MOSFET switching loss not too large, R_g:

$$2 \times R_g \times (Ciss - Crss) \le \frac{Ton\_min}{8}$$

So you can obtain R_g the maximum value in the range, but R_g 's value is as small as possible, because it can reduce the MOSFET switching Loss, thereby it can make the sink size small, but if the R_g is too small, it will result in the shock of driving voltage, and make MOSFET break down.

3. SYSTEM FUNCTION MODULE DESIGN

The study uses a special simulation software for switching power supply Saber, Saber simulation software is a software which is designed by the United States' company Synopsys, it is an EDA software which is hailed as the world's most advanced simulation software, it now become the industry standards software for the simulation of mixed signals, mixed-technology of design and verification tools.

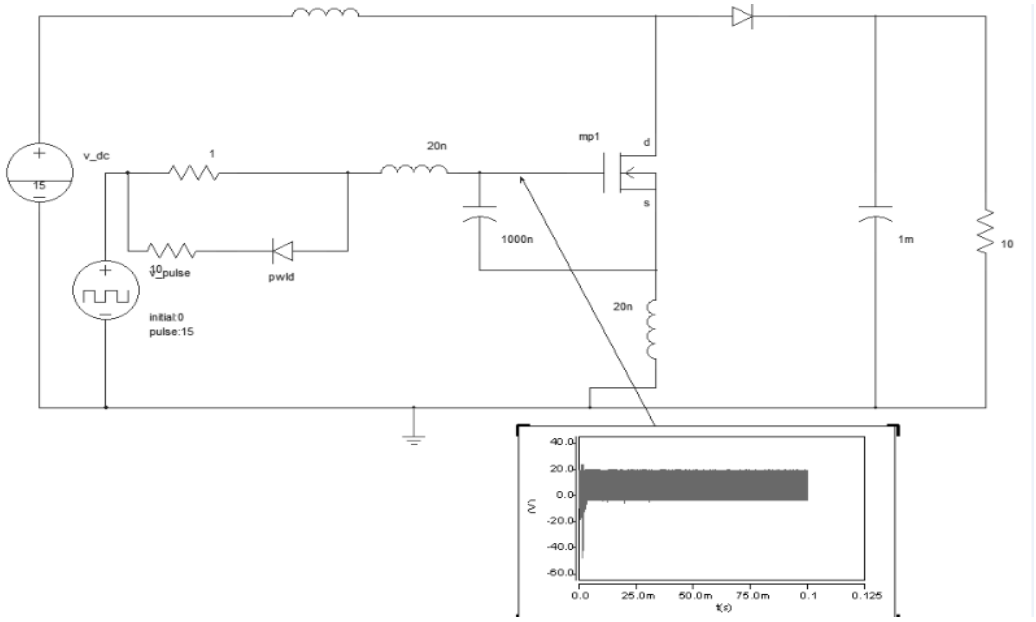

Fig 5: Schematic diagram of Saber simulation

Set the Input capacitance Ciss is 1200(pF), Td(on) opening delay time is 900 (ns), Tr is 300 (ns), Vgs is 15(V), reverse transfer capacitance Crss is 200 (pF).

Saber simulation software occupies a very important role in the research of simulation because of its powerful waveform analysis. There are more than 10 special means of analyzing such as: DC analysis, AC small-signal analysis, Time domain analysis and Frequency domain analysis. The simulation analysis of use Vary embedded time domain analysis.

In the design of PCB Board, the write line length between MOSFET and R_g is about 20mm, its parasitic inductance is 30nH, R_g is from 1 ohm to 28 ohm, the change step is 2.5

ohm, time of simulation is 0.5s, simulation time step is 1us and the drive voltage is 15V, the switch tube driving waveform showed by the figure 6, specific numerical results shows by the table 1.

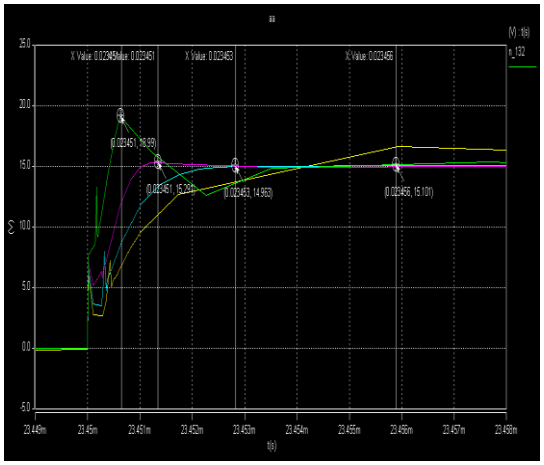

Fig 6: Driving waveform simulation

From the figure, when the parasitic inductance parameter is 30nH and the drive resistance is 10 Ohm, switch tube waveform shocks obviously, and appeared a peak voltage, its peak voltage's maximum value reached 19V, with the increasment of R_g resistance, switch tube waveform shocks has slowed down, when the drive resistance R_g is 24 ohm, waveform becomes flat, and has no shocks, but rising speed of voltage is the slowest, this is due to switch tube MOSFET exists Miller effect (Figure 1 Miller platform stage). If the voltage rises too slowly, it will significantly increase the switching MOSFET's loss, whitch is also a very serious problem.

Tab1: The peak value of shock voltage

Driving resistance	1	10	19	28
Maximum voltage (v)	18.99	15.291	14.963	15.001

The line length is 25mm, the parasitic inductance can be 35nH, R_g value is set from 3 ohm to 27 ohm, the change step of R_g is 3 ohm, drive voltage is 15V, the simulation time is 0.5s, simulation time step is 1us, you can get driving waveform of switches in Figure 7, table 2 is the peak value of driving voltage.

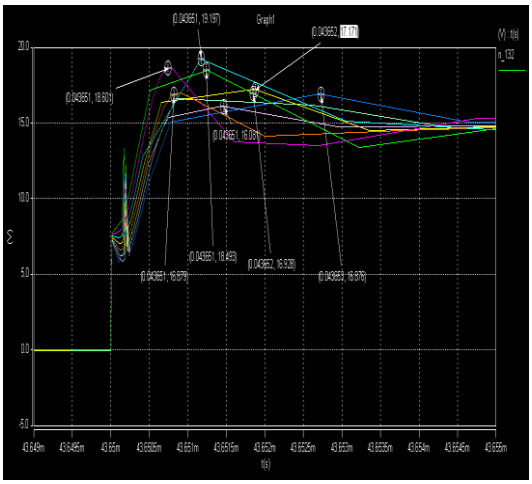

Fig 7: Driver resistance switching waveforms

Table 2 driving resistance under the driving voltage spike peak

Resistance	3	6	9	12
Maximum voltage	18.493	18.601	19.197	18.897
Resistance	18	21	24	27
Maximum voltage	16.928	16.879	16.876	16.081

From the figure, when the parasitic inductance parameter is 35nH and the drive resistance R_g is 10 Ohm, switch tube waveform shocks obviously, and appeared a peak voltage, its peak voltage maximum value reached 18.493V, with the increasment of R_g resistance, switch tube waveform shocks has slowed down, when the drive resistance is 27 ohm, waveform is flat, and has no shocks, but voltage rose slowly. Compared to the previous case, it shocks more severely, Compared two same R_g, the peak voltage increases about 2V. because of the increasment of driving resistance, the charging time of capacitance increases, 33 Ohm shows the effect in the inhibition of waveform shocks, but it will increase the MOSFET switching losses.

By the preceding switches voltage curves, in order to make the MOSFET present an ideal waveform, and to make it work well. The first thing is the attention should be drawn when draw the PCB, the drive circuit's parasitic parameters can influence MOSFET's switch, the write line should be as short as possible. Various factors should be taken into account in selecting the driving resistance, such as: inhibition of switching waveform shocks, inhibition of spiking peak voltage, the MOSFET's minimum turn-on time.

4. SYSTEM TEST AND ANALYSIS

FQA28N50 is used in this experiment, the specific parameters: input capacitance Ciss is 4300(Pf), Td (on) turn-on delay time is 210 (ns), Tr is 250 (ns), Vgs typical voltage is 15 (V), reverse transfer capacitance Crss is 80 (pF).

The formula:

$$R_g \le \frac{Tr + \mathrm{Td}_{(on)}}{16 \times (Ciss - \mathrm{Crss})}$$

$$R_g \le 11.42$$

$$R_g > 2\frac{\sqrt{LC}}{C}$$

$$R_g > 2.383$$

PCB line length is 12mm, the output PWM's duty is 0.5, switching frequency is 20KHz, the driving resistances are 1 ohm, 10 Ohm, 15 ohms, 20 ohm, 50 ohm.

Waveform analysis:

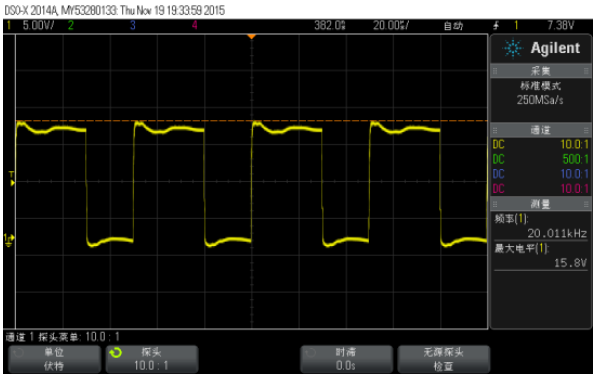

Fig 7: The drive waveforms when the R_g is 20 ohm

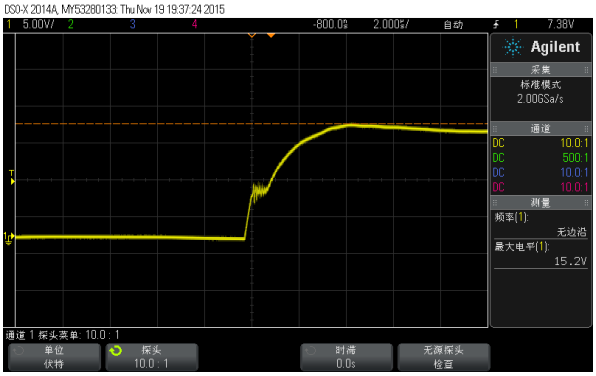

Fig 8: The drive waveforms when the R_g is 50 ohm

Tab 3: The peak value of driving voltage under different value of R_g

Resistance	1	10	15	20	50
Peak voltage (v)	17.2	16.2	16	15.8	15.2

5. CONCLUSION

From the analysis data in charts and tables, the switching frequency is 20KHz, it will have a little shock when resistance is 50 ohm, but can be turned on for the longest time; when the resistance R_g is1 ohm, it have the biggest peak voltage spikes, but the time of opening is the shortest. Combined with the peak voltage spikes and turn-on switching losses two factors, according to the above formula results R_g can be 11.42ohm, take the electromagnetic interference EMI into account, the resistance is larger than 11.42 ohm.

In order to finish a driving circuit design, first it must start with the principle of circuit, under different applications the driving circuit's design principles will be definitely different. When you select the MOSFET, it Should be combined with the circuit voltage and other specific parameters, different switch tube usually have different size of its gate source capacitance, so its corresponding drive resistance Rg is also different. it should be combined with the circuit's voltage and over current specific parameters such as size and enough quantity of selected, different switches its mixed with varying amounts of capacitance between gate and its corresponding driver resistance is also different. When people draw the PCB Board, it should give full attention to driving circuit between the end line to the MOSFET's, its length should be as short as possible under PCB layout allows, usually the length is about 10-15mm, so it can reduce parasitic parameters caused by PCB. Different alignment, And different lenth of PCB walk line, which has the corresponding matching resistance, it is necessary to avoid the shock of the circuit and reduce the switching loss , and achieve the optimization of driving resistance, so as to achieve the purpose of optimizing the driving circuit.

6. REFERENCES

[1] Wang Zhaoan, Liu March. Power electronics [M]. Beijing: China machine press, 2000.30-34.

[2] Shi Xiude. Parasitic parameters of circuit for BOOST converter switches [D]. Harbin Institute of technology, 2012:31

[3] Mei Jun, Zheng Jianyong. Saber simulation model and its application IGBT1 in the solid state switch [J]. Electric power automation equipment.2005 (06): 53

[4] Yin WenChun. DC servo system Study on the application of PWM power amplifier [D].Graduate school of the Chinese Academy of Sciences (Changchun Institute of optical precision machinery and physics), 2004:29-32

[5] Mu Xinhua, Yang Zhiyong. Switching power supply printed circuit board study on the effects of parasitic parameters[J]. Journal of electrical engineering, 2004,24 (11): 121-125.

[6] Xu Chen min, Xu Dehong. SiC MOSFET drive circuit and experimental analysis of [J]. power, 2013 (05): 71

[7] Zhao Q, Stojcic G. Characterization of Cdv/dt induce power loss in synchronous buck DC-DC converters[C]. Applied Power Electronics Conference, Nineteenth Annual IEEE, 2004, 1: 292-297.

[8] Ji Shengru, caught up. MOSFET's isolated high-speed drive circuit [J]. Electric welding machine, 2013 (37): 6-7

[9] NI Yong, Xu Zhen, etc. A parasitic parameter extraction model and optimization of PCB design [J]. the computer measurement and control, 2010,18 (3): 677-681

[10] Cui Yongsheng, Wang Shishan, On the effects of parasitic parameters on characteristics of EMI filter high frequency output simulation [J]. China electro-technical Institute of power electronics society 11th annual meeting, 2008:1-5

[11] Wu Fengjiang, Sun Li. Electromagnetic interference and suppression of bridge-type power MOSFET [J]. University of Aeronautics and Astronautics journal, 2005,37 (1): 29-33