

An Approach to Increase the Effectiveness of Electronic Devices by Reducing Thermal Generation of Current

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ABSTRACT

In this paper we will do the analysis of the gate engineering impact on tri state inverter performance for the application on SOC that is system on chip with the help of different high dielectric material. The high dielectric materials used in electronic circuits for preventing tunnelling effect which will increase the thermally generated current. In order to reduce the Thermally generated current occurs in electronic circuit we can replace the SiO_2 with different materials having high dielectric constant. Tri State Inverter is designed by the use of microwind tool or simulator. The performance of Device is analyse for various parameter. It is measured that by the use of high dielectric constant material in Tri State Inverter the thermally generated current and dissipation of power minimised and also the performance of the circuit gets high. Among various high dielectric constant material, Lanthanum oxide La_2O_3 gained focus due to its property such as High Energy Band Gap, High Dielectric Constant, and can resist upto high Temperature.

Keywords

Tri State Inverter, Low Power, High k, CMOS, VLSI, TG Current.

1. INTRODUCTION

From several years Silicon di Oxide is being used as a Gate oxide material because of its highly cross linked three dimensional structure. As the size of the transistor is reduced the width of the silicon di oxide gate has rapidly decreased. Therefore the gate capacitance get high and thus drive the current and improve the circuit performance. As the width of the Gate oxide lies below 2.0 nm due to tunnelling effect thermally generated current get high which occurs unwanted power consumption and abridge the reliability of device.

The Gate capacitance is increased by changing silicon di oxide gate dielectric with a different high dielectric material with the help of which high physical thickness can be achieved without the thermally generated effects.

We can introduce the material having high dielectric constant instead of SiO_2 gate dielectric and the effect of this high dielectric on the TRI STATE inverter will be analyse. TRI STATE Inverter is designed with the help of two semiconductor materials and six various high k materials and the performance of the circuit will be analyse for different parameter.

In modern semiconductor circuitry Insulator with high dielectrics plays critical role therefore for designing TRI STATE Inverter SiO_2 is not a favourable to be used as a gate oxide. From here we can say that High dielectric materials are best substitutes for gate oxide to enhance the performance. A lot of materials having high dielectric constant has been suggested

There are several requirement for gate dielectric materials among which capacitance performance and good insulating properties are important.

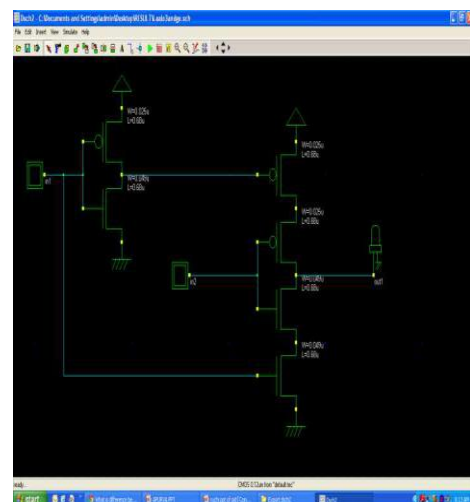
Depends on above mentioned specifications and requirements for high dielectric materials, Different materials of high dielectric constant taken for Analysing Three State inverter. For the gate Insulator the necessary Band Gap for the gate insulator lies in between 5.15 eV to 7.80 eV. For the SiO_2 the band gap is 9.0 eV which is large. Similarly for the La_2O_3 the band gap is 5.8 this band gap is lesser than the above mentioned Band Gap Range. In our Dissertation SiO_2 gate insulator is changed with the different high dielectric materials and Simulation are carried out for three state inverter to evaluate its performance.

A Comparison Table For Different High Dielectric Materials With Silicon Di Oxide Material SiO_2

Dielectric Material	Value of Dielectric Constant(K)	Energy Band Gap inEV
SiO_2	K=3.9	9.0
Si_3N_4	K=7.5	5.30
Al_2O_3	K=9	6.0
Ta_2O_5	K=22	4.40
HfO_2	K=25	5.60
La_2O_3	K=30	5.80

2. TRI-STATE INVERTER

One p-MOS and One n-MOS transistor are used for designing a CMOS inverter. 0 and 1 are the only two logical symbols, when several inverter share a particular node (bus structure), problem will arise hence to avoid multiple access at the same time tri-state inverter are used, featuring the possibility to remain in a "high impedance" state when access is not necessary. It consist of an enable control circuit and a logic inverter as long as the enable En is set to its lower value (0) the output remains in high impedance.



Schematic Diagramme of Tri State Inverter

Truth Table for three state inverter

In	En	Out
0	0	X
0	1	1
1	0	X
1	1	0

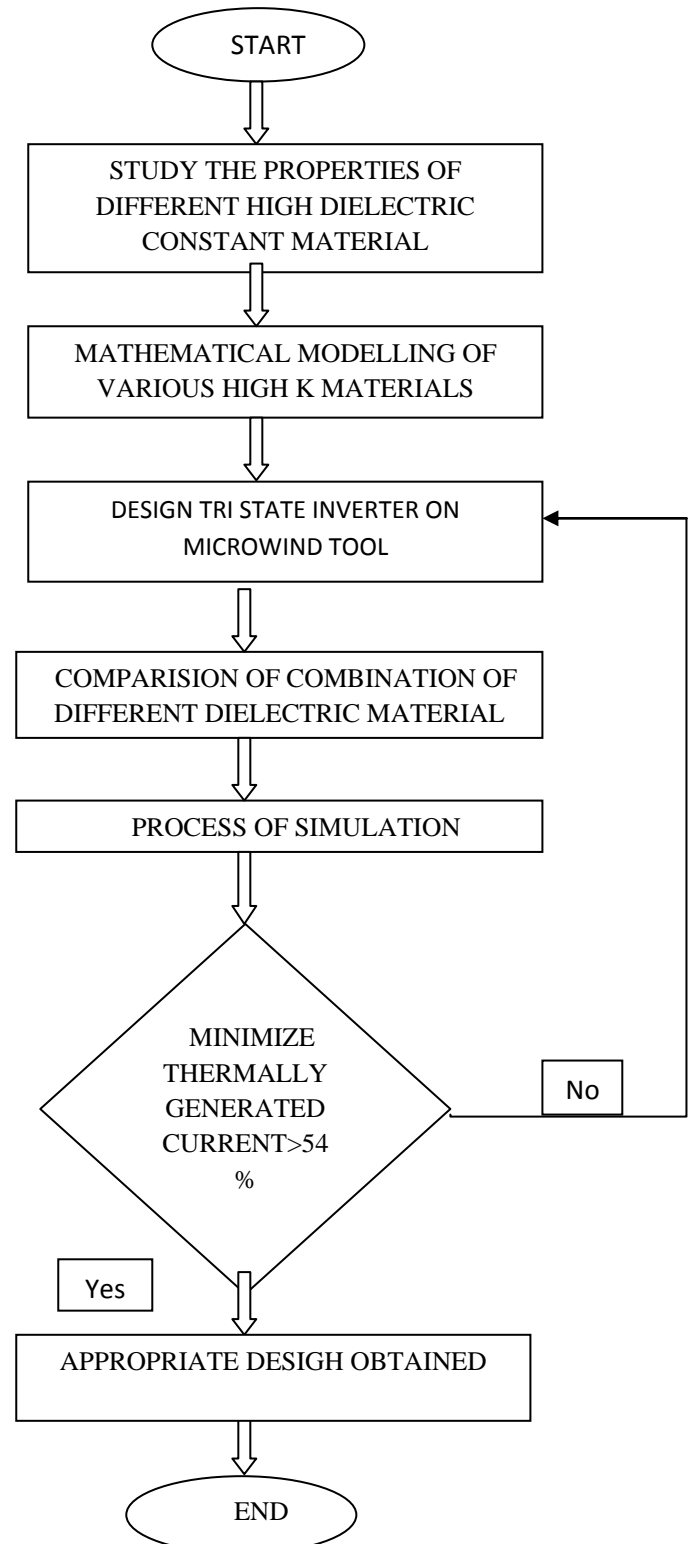
Ordinary complementary metal oxide semiconductor inverter is not connected directly to Vdd and Vss supply. Whenever the cell is disabled, p MOS and n MOS devices are inserted for disconnecting inverter. When En =1 (enable is 1) the cell works as Regular inverter (CMOS Inverter) , but when En=0 (Enable is 0) the outcome is unpredictable in nature or it 'floats' and generates fluctuation at input also generate leakage.

The main sources for generation of thermally generated current are:

1. Drain/Source junction thermally generated current.
2. Thermally generated current due to Direct gate tunnelling.
3. By the channel of an OFF transistor sub threshold leakage occurs.

3. PROPOSED METHODOLOGY

The procedure by which the task is carried out can be presented via FLOWCHART:



Step 1: At the first stage we have study the property of Different Dielectric Material.

Step2: In the Second Stage we do the modelling of Different High k Material mathematically.

Step 3: In the Third stage we have Designed the Tri State Inverter by the use of different high k material on microwind.

Step 4: In the fourth step, combination of dielectric material has compared.

Step 5: we simulate the tri state inverter designed by different Dielectric.

Step 6: check simulation output and compare thermally generated current with the previous outputs.

Step 7: If the thermally generated current minimization is more than previous current then designing of inverter is final other wise we will repeat the step 3.

4. SIMULATION AND PERFORMANCE EVALUATION

We have introduced several methods to minimize the thermally generated current of the circuit of the device, in the first part of the Paper. Our methodology does not require any kind of modification in technology processing, therefore they can easily be used. Then We presents the technique for minimization of thermally generated current of tri state inverter by the use of high K materials. Results shows that by the use of our proposed method thermally generated current decreased up to 87.2 %.

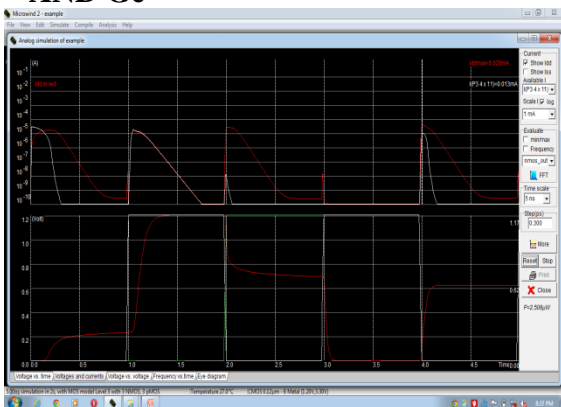
The simulation process is done with a different dielectric constant having value of 3.9,7.5,9.0,22.0,25.0,30.0. These Value of Dielectrics correspond SiO₂,Si₃N₄,Al₂O₃,Ta₂O₅,HfO₂,La₂O₃. In every simulation, La₂O₃ have minimum thermally Generated current and SiO₂ have maximum thermally generated current.

The Tri State Inverter gives the decrement in thermally generated current by about 87.2%. This improvement has been done because drain current has attributed to increased electron velocity at source end. Thus transport efficiency of the carrier enhance.

In our Work sio₂ gate insulator material is changed by another high k material and simulation has been done. The thermally generated current of Tri State Inverter ,plotted for different high k materials in Diagramme.

Thermally Generated current of the circuitry designed by SiO₂ as a dielectric is 0.054mA. It can observed from the output images that as the value of gate dielectric gets high Thermally generated current Reduced in an Exponent way because dielectric materials provide high physical thickness hence reduced tunnelling effect through insulator. Thermally generated current of device designed by La₂O₃ as Dielectric is 0.013mA which shows a decrement of about 87.2% as compared to thermally generated current produced by SiO₂ as a dielectric.

5. SIMULATION RESULT OF LA2O3 AND Ge



6. CONCLUSION

We are able to conclude that Germanium and Lanthanum are best material among the other used material. They provides optimum results under the similar condition. In our work we mainly considered different high dielectrics and try to find optimum result and get rid the problem of thermally generated current.

It has observed that the leakage in the circuitry is decreased by 87.2% as the value of k increased from 3.9 (SiO₂) to 30 (La₂O₃) makes the circuitry to be able to work without consuming more power, It also produce low thermally generated current and provide high efficiency. Therefore the Tri State Inverter with High k as the gate Dielectric material can used in low power applications and can also be considered as a prominent device for future electronic market and semiconductor industry.

7. REFERENCES

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