High Speed 32-bit Vedic Multiplier for DSP Applications

Arunkumar P. Chavan
Asst. Professor,
Department of ECE
RVCE Bangalore, INDIA

Rahul Verma
Student,
Department of ECE
RVCE Bangalore, INDIA

Nishanth S. Bhat
Student,
Department of ECE
RVCE Bangalore, INDIA

ABSTRACT
Digital signal processing typically requires large number of mathematical operations to be performed repeatedly on the samples of data with less delay and power consumption. Multiplication is the fundamental arithmetic operation and determines the overall execution time of the processor. In this paper two high speed 32-bit Vedic multipliers are designed based on Urdhva-Triyakhbhyam sutra. Addition of partial products of proposed multipliers is done using Kogge stone adder and ripple carry adder respectively. Proposed multiplier-1 and proposed multiplier-2 were compared with the one with the highest speed and a reduction of 77% and 65.37% is achieved respectively. The coding is done using Verilog HDL and synthesized using cadence too**l.**

Keywords
Vedic Mathematics, Urdhva Triyakhbhyam, Kogge Stone Adder, High Speed.

1. INTRODUCTION
Signal processing plays a crucial role in a many applications ranging from mobile communication to pattern recognition. The key parameters of a Digital Signal Processor are low power, high Speed and small area. Multiplier is the most important component of a DSP and accounts for a large portion of the overall delay in the processor. Several multiplier architectures have been proposed like Array multiplier[1], Sequential multiplier[2], Booth's multiplier[3], Dadda's multiplier [1]etc.

Parallel multipliers can be categorized as array based and tree based multipliers. The add and shift multiplier [1] is an example of an array multiplier. It has a simple structure but consumes more area and leads to higher power consumption. Booth multiplier [3] was designed which requires less area but cannot work when it has alternate zeros and ones. Wallace tree multiplier [1] is a tree based multiplier which has high speed but it suffers due to irregularity in structure. Hence a high speed and area efficient multiplier is made using principles of Vedic mathematics.

In this paper there are two proposed multipliers. Proposed multiplier-1 is designed using kogge stone adder and proposed multiplier-2 is designed using ripple carry adder. The proposed multiplier is implemented in 45nm process technology and compared with conventional multipliers [4] with respect to timing, area and power. The design is synthesized using Cadence RTL Compiler and is imported into Cadence Encounter Tool and the final layout has been obtained.

The outline of the paper proceeds as follows: section 2 gives an overview of Vedic mathematics and urdhva-triyakbyham sutra. Section 3 provides the detailed design of the multiplier architecture and its various sub components. Section 4 deals with the design and working of the kogge stone adder and ripple carry adder used in proposed multipliers. Section 5 focuses on the layout and measurement results, section 6 presents the conclusion of the proposed multipliers.

2. OVERVIEW OF VEDIC MATHEMATICS AND URDHVA-TRIYAKBYHAM SUTRA
VEDIC mathematics is an ancient form of Indian mathematics that was extracted from ancient sculptures (Vedas). The term 'VEDIC' is originates from the word "Veda" which means "Store House of Knowledge" [5].The algorithms used in conventional mathematics can be optimized for faster operation using Vedic mathematics, making it a suitable choice for implementation of High speed arithmetic circuits. It finds applications in diverse fields like trigonometry, plain and spherical Geometry, calculus, conics etc.

Vedic mathematics can be completely described based on 16 sutras. Among them Urdhva-Triyakhbhyam and Nikhilam Navatascaramam Dasatah sutra is used for multiplication operation. The main advantage of a multiplier based on urdhva-triyakbyham sutra is that with the increase in number of bits, the corresponding increase in area and timing is much slower when compared to other multiplier designs [6]. The Vedic multiplier proposed performs multiplication based on Urdhva-Triyakhbhyam sutra.

2.1 Urdhva-Triyakhbhyam" (UT) Sutra
The literal meaning of Urdhva-Triyakhbhyam is "vertically and crosswise", as the format of multiplication proceeds in a similar fashion [5]. The UT sutra reduces latency of the multiplier unit by generation of partial products in parallel. A line diagram illustrating the working of UT sutra for binary multiplication is shown in Fig.1. The vertical and crosswise lines indicate the generation of partial products.

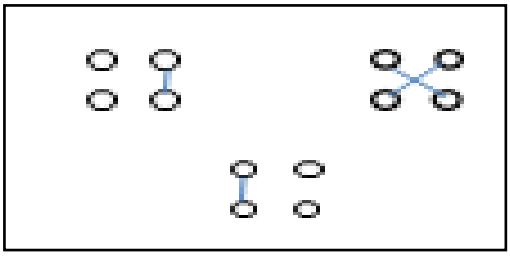

Fig.1: Line Diagram for multiplication of two 2-bit numbers

3. DESIGN OF THE MULTIPLIER ARCHITECTURE AND ITS VARIOUS SUB COMPONENTS
The operation of UT sutra for a 2-bit multiplier is shown in fig.2. Consider two numbers A=A1A0 and B=B1B0 of 2 bits each. First the Least Significant bits (LSB) of A and B i.e. A0 and B0 are multiplied and the LSB of output S [0] is obtained. The second step is to take the products in a crosswise manner

(A1B0 and A0B1) and pass it as inputs to the half adder. The sum bit of the half adder corresponds to S [1] and carry bit serves as carry input to the next half adder.

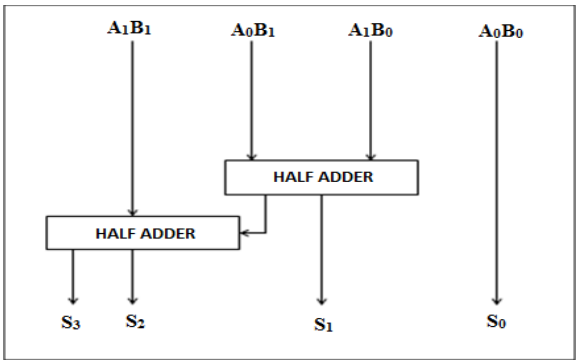

Fig.2: Architecture of a 2x2 Vedic Multiplier

The next step is to multiply the most significant bits (MSB) A1 and B1 and compute their sum with previously obtained carry. The sum output is S [2] and carry gives the fourth bit of final result. Final output obtained is C [2] S [2] S [1] S [0].

S0 = A0 B 0 (1)
C1 S1 = A 1 B0 + A0 B1 (2)

C2 S2 = C1 + A1 B1 (3)

The same principle can be used to design Vedic multipliers with increase in bit length. The architecture of 32-bit Vedic multiplier using four 16-bit Vedic multipliers and three 32-bit adders is designed and shown in the fig 3.

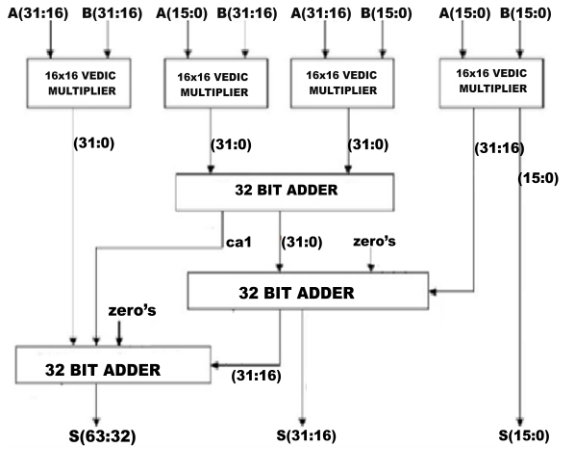

Fig.3 Architecture of 32x32 Vedic Multiplier

Consider two 32-bit numbers A [31:0] and B [31:0].Let the final product be denoted as S [63:0]. A [15:0] and B [15:0] are multiplied using a 16-bit Vedic multiplier to obtain P [31:0]. P [15:0] corresponds to the output S [15:0]. P [31:16] is added to the result of addition of A [15:0] * B [31:16] and A [31:16] * B [15:0].The rightmost 16 bits of the adder output gives S [31:16]. The remaining 16 bits are added with product of A [31:16] and B [31:16] along with carry to give the output S [63:32].

4. DESIGN AND WORKING OF THE KOGGE STONE ADDER AND RIPPLE CARRY ADDER USED IN PROPOSED MULTIPLIERS

4.1 Kogge Stone Adder (KSA)

KSA is one of the fastest adder designs for high speed arithmetic circuits. It is a parallel prefix form of the carry look-ahead adder, as generate and propagate signals is pre-computed. The main factor for its high speed is that carries are computed in parallel which reduces logical depth and has bounded fan-out. Carry is generated in O (log n) time. The KSA prefix network has built in redundancy which can be utilized for fault tolerant designs [7].

The working details of KSA are explained in terms of three distinct stages:

i. Pre-processing (P and G generation)

ii. Look-ahead carry generation (CPi and CGi generation)

iii. Post processing (Computation of Sum)

4.1.1 Pre-Processing

Pre- Processing stage produces the generate (Gi) and propagate (Pi) signals for each pair of bits corresponding to the inputs (Ai and Bi).The Boolean equations are

Pi=Ai xor Bi

Gi=Ai and Bi

4.1.1.1 Look-ahead carry Generation (LCG)

LCG stage is responsible for the high performance of the KSA and makes it better than other designs. LCG involves computation of carries corresponding to each bit. The operations are done in parallel and hence deliver high speed. It makes use of carry propagate and generate signals as intermediate signals. The logic equations are

CPi:j= Pi:k+ 1 and Pk:j
CGi:j= Gi:k+ 1 or (Pi:k+ 1 and Gk:j)

4.1.1.2 Post-Processing

Post processing is the final stage of computation. It is used by all adders belonging to the family of Carry-look ahead adders. It involves generation of sum bits given by the logic equations:

Ci– 1 = (Pi and Cin) or Gi
Si = Pi xor Ci– 1.

Working of 8-bit kogge stone adder is shown in the fig.4. The proposed multiplier uses 32- bit KSA.

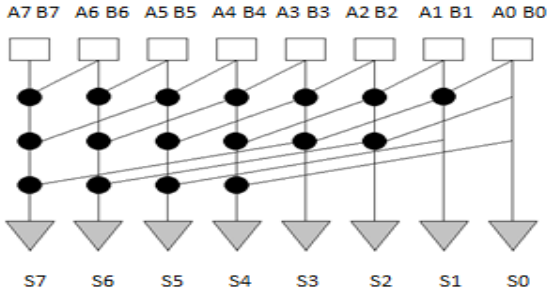

Fig.4 Structure of 8-bit Kogge Stone Adder

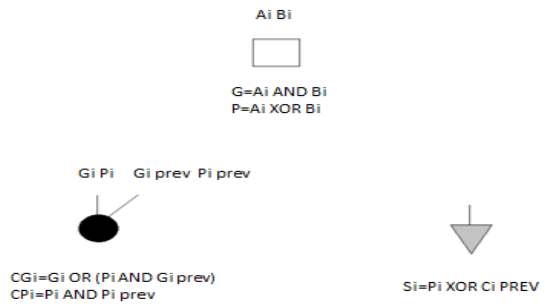

Fig.5 Components of Kogge-Stone Adder

4.2 Ripple Carry Adder

Ripple carry adder has a simple structure. It consists of a cascade of full adders, with the carry output of each full adder given as carry input to the next adder in a chain-like fashion. The Most Significant Bits (MSB) of the sum output cannot be obtained unless the carry signal has rippled through the full adders from the Least Significant Stage to the Most Significant Stage. There is considerable delay in computation of final Sum and output carry. Hence it is slower than Kogge Stone Adder, which is based on computation of carry signals in parallel.

5. LAYOUT AND MEASUREMENT RESULTS

Proposed multiplier-1 and multiplier-2 are designed, simulated, synthesized and physical design is carried out in 45 nm process technology using Cadence environment. The delay comparison of the multipliers is shown in Table 1.

TABLE 1. The Experimental results comparison between the proposed design with others.

Multiplier design	Width of the multiplier	Delay (ns)
Proposed Design -1	32	0.95
Proposed Design -2	32	1.43
Design in [8]	32	9.54
Array multiplier [1]	32	20.64
Wallace tree multiplier[1]	32	11.6
Dadda multiplier [1]	32	10.97
Reduced Area multiplier [1]	32	12.03
Radix-4 booth multiplier[1]	32	12.27
radix-8 modified booth multiplier[8]	32	12.081
radix-16 modified booth multiplier[8]	32	11.564
Design in [9]	32	4.13

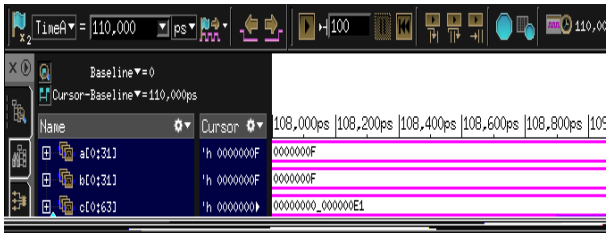

Fig.6 Shows the simulation waveform for the proposed multipliers.

Fig.7 shows the plot for delay of different multipliers. From the plot it can inferred that proposed multiplier-1 and proposed multiplier-2 have less delay compared to other designs.

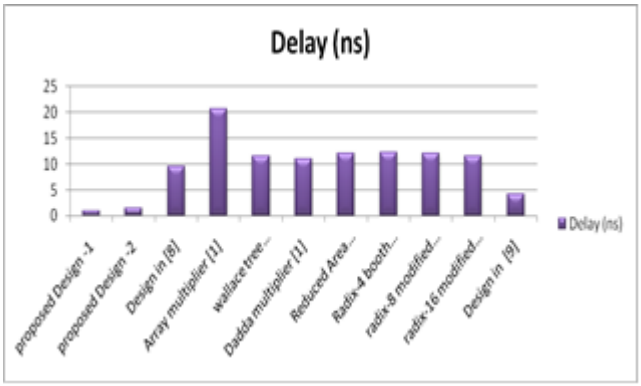

Fig.7 Delay comparison of multipliers

The physical layout of the proposed multiplier is shown in the Fig.8.

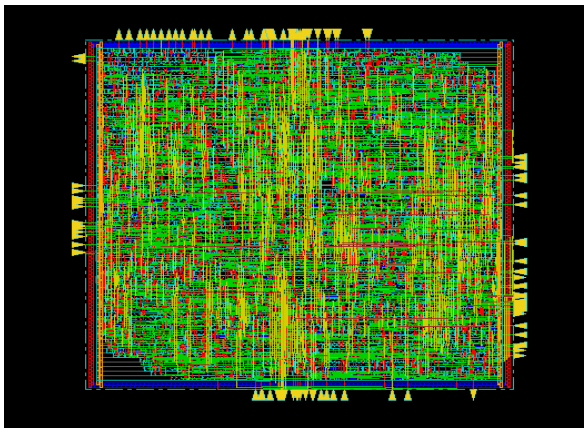

Fig.8 Chip layout for 32*32 Vedic multiplier

6. CONCLUSION

Alternate design of multiplier cell were designed and compared. The proposed multiplier -1 and multiplier-2 were built using kogge stone adder and ripple carry adder respectively. The multipliers were modeled in verilog HDL and synthesized Using Cadence Digital Complier (DC) under 45nm standard cell library. The synthesized netlists were loaded into Cadence SOC Encounter to carry out RTL to GDSII code. Due to the advantage of processing time, the proposed multipliers can be used in high- speed applications

7. REFERENCES

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