Improving Error Correction Capability of Aggressive Packet Combining Scheme by using Half-Byte Packet Reverse Technique and Even - Odd Selection Method

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ABSTRACT
Aggressive Packet combining scheme is very efficient technique for error correction in wireless data communication. Transmitter transmits three copies of the original packet. Receiver applies bit by bit majority voting on the received erroneous copies and gets the original packet.

The major limitation of APC is that, if the bit error occurs in the same bit location of all the received copies then APC fail to correct them which results in reduced correction capability and reduced throughput. In this paper, a new modified APC technique is proposed that can eliminate the major limitation of the APC by using half-byte packet reverse technique and even & odd selection method thus increasing correction capability and throughput.

General Terms
Correction capability, odd-even selection, packet reverse technique.

Keywords
Aggressive packet combining (APC), bit wise majority logic, packet reverse packet combining scheme, even &odd selection.

1. INTRODUCTION
A major challenge faced by the researcher is to transmit the data from transmitter to receiver successfully. Practically the channels are not stable all the time thus, erroneous packet are received at receiver side. Two techniques i.e. Forward Error Correction (FEC) and backward error correction are used for reliably transferring data from sender to receiver. In BEC retransmission technique is used for error correction thus, transmission delay occurs. Backward error correction is suitable for the wired transmission. Forward error correction is suitable for the wireless communication where error correction codes are used for detection and correction of error if any. Leung [1] proposed an idea of Aggressive Packet Combining scheme (APC) for error control in wireless networks with the basic objective of fast error control in relatively higher noisy wireless networks**.** In APC, three copies of a packet is transmitted from source node to destination node. If all the received copies are erroneous, bit by bit majority voting is applied to get the correct packet. A major drawback of APC is that if error occurs in same location of erroneous copies of a packet then the application of majority logic fails to get original packet. Several modifications of APC are reported in [2-8] to increase throughput, tackling various error syndromes and enhancing fast correction.

In this paper, the modified APC technique is proposed to overcome the problem of conventional APC (if the error occur in same bit location of all the received copies, then APC fail to correct them) by using half-byte packet reverse at 2nd copy and even /odd selection method at 3rd copy. Theoretical analysis shows that the proposed scheme has better error correction capability than the conventional APC.

2. REVIEW OF HALF-BYTE PACKET REVERSE SCHEME AND APC

2.1. Half-Byte Packet Reverse Scheme
The idea behind Half-Byte packet reverse scheme was taken from Packet Reverse Packet Combining scheme (PRPC) [9-10]. In this scheme, each half-byte of packet is separately reversed and combined and then transmitted. Receiver side applies the same phenomena to decode the received packet. Let us understand this by considering an example:

Let the original packet is 10101100

Transmitter:

Table 1. Half-Byte Reverse at Transmitter

First half byte reverse=1010	0101
Second half byte reverse = 1100	0011

Transmitter transmits: 01010011

Receiver side: Erroneous copy as 0101**1**011 (Bold face shows error bit) and applying reverse phenomena we get as table 2.

Table 2. Half-Byte Reverse at Receiver

First half byte reverse	1010
Second half byte reverse	110**1**

Now receiver has **10101100** and is the original packet.

2.2 Aggressive Packet combining scheme
Aggressive packet combining scheme is a modification of MjPc (Majority Packet Combining) [11]. In APC three copies of the original packet is send from source to destination. If received copies are erroneous then bit-by-bit majority logic is applied on the three copies at receiver side and combined

packet is again applied to error detection test. If it is found to be erroneous then least reliable bits are identified. And correct bit pattern for these bits are again searched. All the generated copies are again applied for error detection and if correct packet is obtained then next packet is requested, if not correct then retransmission is requested for same packet. Figure 1 shows an example.

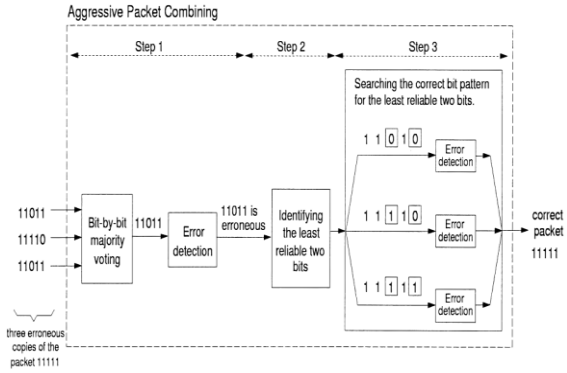


Fig. 1: Aggressive Packet Combining Scheme.

APC fails when error occurs at same bit location in all the copies as in example 3 where error locations are shown in bold face.

Table 4. APC scheme when error is at same location in three copies of 10101 packet (red colored is erroneous bits).

Received Copies	Bit-by-Bit Majority Logic	Error Detected	Least Reliable bits	Search the Correct Pattern	Error Detected
11111	11101	Yes	1st and 2nd bit from right	11111	Yes
11101				11110	Yes
11100				11100	Yes

3. PROPOSED SCHEME

As it is likely in wireless transmission that three copies transmitted at a time will have the same link error syndrome resulting into all three copies having error at same bit position(s) [12-13].In order to overcome the drawback (i.e. correction of error when error occurs at same bit location of two or more copies) of conventional APC, new modified technique of APC is introduced for transmission of packet from source to destination. In this modified technique, if the two or more error occurs in the same bit location, then it can be detected and corrected to get the original copy by applying half-byte packet reverse and even & odd selection method. The idea is based on the logic that bit reversal or positional changes in the transmitted copies may reduce the occurrence of double or triple bit error in same location after decoding at the receiver using same logic thus increasing the correction capability. Figure 2 shows the diagram of the proposed scheme and it can be understood as per the diagram in figure 2.

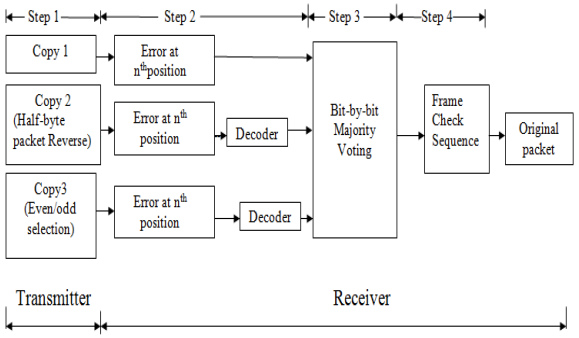


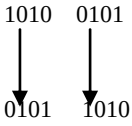
Fig. 2: Proposed Scheme

The main idea of the proposed scheme can be explained by executing the following steps:

<u>At transmitter</u>

Step 1:

- Copy 1 of the original packet is transmitted without any coding.
- Copy 2 is transmitted after applying half-byte packet reverse logic of packet. In this logic packet is divided into two halves and then packet reverse is applied on the two halves and then combined as a single packet and then transmit it to the receiver. It is illustrated as the original packet is 10100101.



Transmitted copy is 01011010.

- Copy 3 is transmitted after applying odd and even selection method where even bits are placed in left side and odd bits are placed in right side of the packet.

<u>At receiver</u>

Step 2:

- Error detection of each copy takes place to detect the presence of errors at the received copies.
- Error detection is followed by decoding of second and third copies.

Step 3:

- Bit-by-bit majority voting is applied on the decoded copy 2, copy 3 and copy 1.

Step 4:

- Copy obtained after step 3 is again applied to the error detection (FCS) to find whether the obtained copy is erroneous or not. If no error is detected then we get the original packet and if error is detected then copies are discarded and request for retransmission of the packet.

Let us understand the scheme considering various examples as follows:

Example 1: Say the original copy is 10100101.

- First copy, C_O = 10100101, it is received with error in 2nd position from left as C'_O = 11100101
- Second Copy with Half-byte packet reverse, C_{HPR} =01011010. It is received with error in the same bit position as that of the first copy as C'_{HPR} = 00011010. Receiver decode the received copy using the same logic and get the copy as C'_{HPR} = 10000101.
- Third copy with even-odd bit selection, C_{EO} =00111100 (blue colored are even bits and black colored bits are odd). It is again received with error at same position i.e. 2nd bit form left side as C'_{EO} = 00111100. Receiver decode the copy using same logic and get the copy as C'_{EO} = 10100101.
- Apply bit-by-bit majority voting on all the three copies and get the result. Apply error detection on the obtained copy to find whether obtained copy is correct or not. If correct, next packet is requested. If not, retransmission is sought. Whole procedure is presented in tabular form:

Example 2: Original packet is 10100101

Table 5. Proposed scheme for the packet 10100101

Transmitter	Receiver			
	Received Copy	Decoded copy	Bit-by-Bit Majority logic	Error Detection
C_O: 10100101	11100101	11100101	10100101	No (10100101= Original copy)
C_{HPR}: 01011010 (Half-Byte Packet Reverse)	00011010	10000101		
C_{EO}: 00111100 (Even-odd selection)	00111100	10110101		

Example 3: Original packet is 00101010

Table 6. Proposed scheme for the packet 00101010

Transmitter	Receiver			
	Received Copy	Decoded copy	Bit-by-Bit Majority logic	Error Detection
C1: 00101010	00111010	00111010		
C2: 01000101 (Half-Byte Packet Reverse)	01010101	10101010	00101010	No (00101010= Original copy)
C3: 00000111 (Even-odd selection)	00010111	00101011		

Example 4: Original packet is 11011011.

Table 7. Proposed scheme for the packet 11011011

Transmitter	Receiver			
	Received Copy	Decoded copy	Bit-by-Bit Majority logic	Error Detection
C1: 11011011	10011011	10011011	11011011	No (11011011 =Original copy)
C2: 10111101 (Half-Byte Packet Reverse)	11111101	11111011		
C3: 11011011 (Even-odd selection)	10011011	11001011		

Example 5: Original packet is 10110011.

Table 8. Proposed scheme for the packet 11011011

Transmitter	Receiver			
	Received Copy	Decoded copy	Bit-by-Bit Majority logic	Error Detection
C1: 10110011	10010011	10010011	10110011	No (10110011 =Original copy)
C2: 11011100 (Half-Byte Packet Reverse)	11111100	11110011		
C3: 01011101 (Even-odd selection)	01111101	10110111		

Example 6: Original packet is 00110011.

Table 9. Proposed scheme for the packet 00110011

Transmitter	Receiver			
	Received Copy	Decoded copy	Bit-by-Bit Majority logic	Error Detection
C1: 00110011	01110011	01110011	00110011	No (00110011=Original copy)
C2: 11001100 (Half-Byte Packet Reverse)	10001100	00010011		
C3: 01010101 (Even-odd selection)	00010101	00100011		

With the above examples it is illustrated that modified APC with half-byte packet reversed and even-odd selection copy can correct errors which occur in the same bit position in all the received erroneous copies, and also the burst error which occur in regular pattern.

4. RESULTS AND ANALYSIS

The proposed scheme has many desirable properties:

- The proposed scheme can perform some error corrections while it does not add additional bits to the packet. This is different from the traditional concept of forward error correction. Consequently, the proposed scheme does not consume extra bandwidth in the wireless channel.
- As in conventional APC, when error occurs in same location of all the received copies it fails to correct the packet. But with this proposed scheme errors get distributed with the decoding process and we can get the correct packet. As a result correction capability of APC is increased.

In the conventional APC scheme, three copies of a packet is sent and when double bits and single bit error occurs then the correction capability is not affected and it can correct the errors at the receiver side without requesting for retransmission. If P1, P2 is the probability of packet with single bit and double bit respectively, then it is given by [14]:

$$P1=kC1\alpha1\ (1-\alpha)k-1 \quad \text{---------- (1)}$$

$$\text{And } P2= kC2\ \alpha2\ (1-\alpha)k-2 \quad \text{---------- (2)}$$

Where k is the packet size, α is bit error rate.

Thus probability of packet in error except double bit and single bit error is given by:

$$P'=P- P1- P2 \quad \text{---------- (3)}$$

And correction capability of APC is given by:

$$CAPC= (1- P') \quad \text{---------- (4)}$$

Thus, throughput efficiency of APC with double bit error is given by:

$$\eta APC = (3P2+ (P'/ (1-P'))) \quad \text{---------- (5)}$$

where P'=P- P1- P2 and the first part of equation (5) is for conventional APC for correcting double bit error; second part is for normal stop-and-wait ARQ other than double bit error and single bit error.

In the modified technique, the probability of single bit error, double bit error and triple bit errors will be corrected as follows:

If P1, P2 and P3 are the probability of packet with single bit, double bit and triple bit error respectively, then receiver will acknowledge without these error is:

$$P= P1 + 2P2+3P3 \quad \text{---------- (6)}$$

Thus, probability of packet in error except single bit, double bit and triple bit errors is given by:

$$P'' = P-P1-P2-P3 \quad \text{---------- (7)}$$

Where P1, P2 and P3 are the probability of packet with single bit, double bit and triple bit error respectively and P1, P2 is given as in equations (1) and (2) and P3 is given as

$$P3= kC3\ \alpha3\ (1-\alpha)k-3 \quad \text{---------- (8)}$$

And correction capability of modified APC scheme is given by:

$$CMAPC= (1- P'') \quad \text{---------- (9)}$$

Thus, throughput efficiency or average number of times a packet needs transmission (including retransmission) for successful delivery with triple bit error is given by:

$$\eta MAPC = (P1+2P2+ 3P3+ (P''/(1-P''))) \quad \text{------ (10)}$$

Where P''=P- P1- P2 - P3 and the first part of equation (10) is for modified APC for correcting triple bit error; second part is

for normal stop-and-wait ARQ with bit errors other than triple bit, double bit and single bit error.

5. CONCLUSION

In the traditional APC, transmitters transmit the three copies of the original packet. If error occurs in these three copies at the same bit location then APC fails to correct it. This limitation is overcome in this paper by using the new technique where half byte packet reversal logic and even and odd selection method is applied. In this paper, it can be concluded that when modification was done using half byte reversal in the second copy and even &odd selection method in the third copy then the improvement in the correction capability of the conventional APC was observed. Thus, throughput increases and bandwidth utilization decreases as number of retransmissions get reduces. In future, simulation results of the proposed technique and conventional APC will be evaluated and compared to show the superiority of the proposed technique over conventional APC.

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