Current Comparison based Domino with Clamped Bit-Line Current Amplifier for Wide Fan-In Gates

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ABSTRACT
A greater part of the low power design methodology is allocated for reducing leakage current. This plays a vital role in static power dissipation. In this project, a current comparison domino pull-up network with its worst case leakage current is compared with Current comparison based Domino (CCD) with Clamped bit-line Current-sensing Amplifier circuit. Thus, the contention current and consequently power consumption and delay are reduced. The leakage current is also decreased by utilizing the footer transistor in diode configuration, which results in increased noise immunity. The simulation results of wide fan-in gates designed using a 16-nm high-performance predictive technology model demonstrates 46 % power reduction and at least 2.36× noise-immunity improvement at the same delay compared to the standard domino circuits for wide fan – in OR gates.

Keywords
Clamped bit-line Current Sense Amplifier, Domino Logic.

1. INTRODUCTION
With newer technologies, power is a primary design constraint. Power dissipation has skyrocketed due to transistor scaling, chip transistor counts and clock frequencies. The power affects packaging costs, chip and system cooler cost, battery life, noise & reliability, environmental conditions and Power supply rail. The CMOS power dissipation has become a very hot topic during the last decade or so. The number of battery powered handheld applications, e.g. mobile phones and laptop computers is steadily increasing and more and more functions are integrated into the systems, e.g. multi-media applications on mobile phones. This is one of the driving forces for analysis of the mechanisms of power dissipation and power-reduction techniques. Another driving force is the incredible power dissipation of state-of-the-art microprocessors where heat removal and current delivery are very hard and expensive to accomplish.

Dynamic/static pair is called domino gate. In dynamic logic, problem arises when cascading one gate to the next gate. In order to cascade dynamic logic gates, one solution is Domino logic, which inserts an ordinary static inverter between stages. Domino only performs non inverting functions that is AND, OR but not NAND, NOR, or XOR. Fast Domino gates are inserted selectively into critical speed paths, with custom SRAMs and optimized synthesized logic, Standard power saving techniques are also used. Domino gates are clocked by multiphase clocks. The operating period of the cell when its input clock and output are low is called the precharge phase or cycle. The next phase, when the clock is high, is called the evaluate phase or cycle. Dynamic logic is normally done by charging and selectively discharging capacitance (i.e. Capacitive circuit nodes). It is classified into precharge and evaluate clock. Precharge clock to charge the capacitance and evaluate clock to discharge the capacitance depending on condition of logic. In CMOS domino logic, when CLK is low, dynamic node is precharged high and buffer inverter output is low and when CLK goes high, dynamic node is conditionally discharged and the buffer output will conditionally go high. It is based on the simple principle that delay variations can be reduced by appropriately tuning the keeper strength and the different principle is exploited to reduce delay variations in domino circuits.

Domino logic circuit techniques are extensively applied in high-performance microprocessors. Conventional standard domino improves noise immunity, it increases current contention between the keeper transistor and the evaluation network. Thus, it increases power consumption and an evaluation, delay of standard domino circuits. Circuit techniques changing the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD) [3], high speed domino (HSD) [4], leakage current replica (LCR) keeper domino [5], and controlled keeper by current-comparison domino (CKCCD) circuit and designs changing the circuit topology of the footer transistor such as diode footed domino (DFD) [2] diode-partitioned domino (DPD) and Current Comparison Based Domino wide fan – in gates of domino CMOS circuits also increases power consumption. [1]

In this proposed technique, Clamped bit line current sensing amplifier is used along with CCD wide fan in the gates. The use of current sensing amplifiers has a number of benefits over voltage sensing amplifiers. The most important ones are significant reductions in bit-line voltage swing and major reductions in sensing delays. These benefits translate to lower dynamic power consumption and increased sensing speed. The key to these improvements lies in the low input resistance of the current sensing amplifier. This becomes evident when examining the equivalent sensing circuit. The current sense amplifier consists of two parts: one is the current-transporting circuit with unity-gain current transfer characteristics and the second are the current sense amplifier that senses the differential current. Due to their great importance in memory performance sense amplifiers have become a very large class of circuits. Their main function is to sense or detect stored data from a read selected memory cell. The memory cell being read produces a current "IDATA" that removes some of the charges (DQ) stored in the pre-charged bit lines. Since the bit – lines are shared by other similar cells, Since the bit-lines are very long, and are shared by other similar cells. The need for increased memory capacity, higher speed, and lower power consumption has defined a new operating environment for future sense amplifiers. Below are some of the effects of increased memory capacity and decreased supply voltage: 1) Increase in the number of memory cells per bit-line increases CBL, while an increase in length of the bit-line increases RBL 2) Decreasing memory-cell area to integrate more memory on a single chip reduces the current IDATA that is driving the now heavily loaded bit-line. This, coupled with increased CBL causes an even smaller voltage swing on the bit-line. 3) Decreased supply voltage results in smaller noise margins, which in turn affect sense amplifier reliability.

2. CURRENT COMPARISON BASED DOMINO FOR WIDE FAN – IN GATES

The circuit shown in figure 2 has five transistors and a shared reference circuit compared to standard footless domino (SFLD). It has two stages. The first stage pre evaluation network includes the PUN and transistors *MP re*, *M*Eval, and *M*1. The PUN, which implements the desired logic function is disconnected from dynamic node Dyn, unlike traditional dynamic logic circuits, and indirectly changes the dynamic voltage.

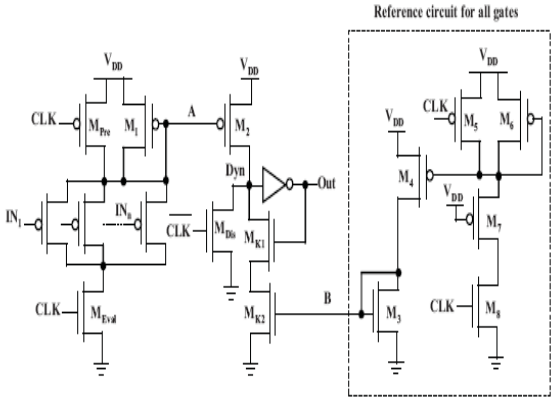

Figure 2 Implementation of wide OR gate using a CCD

The second stage looks like a footless domino, without any charge sharing, one transistor *M*2 regardless of the implemented Boolean function in the PUN, and a controlled keeper consists of two transistors. Only one pull-up transistor is connected to the dynamic node instead of then-transistor in the *n*-bit OR gate to reduce capacitance on the dynamic node, yielding a higher speed. The input signal of the second stage is prepared by the first stage. In the evaluation phase, thus, the dynamic power consumption consists of two parts: one part of the first stage and the other for the second stage. As we know the dynamic power consumption directly depends on the capacitance, voltage swing, and contention current on the switching node in the constant condition of frequency, power supply, and temperature. The first stage with *n*-input has a lower voltage swing *V*DD to *V*THP and no contention. On the other hand, the second stage has rail-to-rail voltage swing with minimum contention. It has some area overhead, it has less dynamic power consumption compared to footless domino.

Transistor *M*1 is configured in diode connection, i.e., its gate and drain terminal are connected together. In the evaluation mode, the current of the PUN transistors establishes some voltage drop across *M*1. This voltage will be low, if all inputs are at the highest level and only leakage current existing in the PUN and mirror transistor *M*2. Otherwise, if at least one conductive path exists between node A and ground, for example, the level of one input becomes low in the OR gate, this voltage drop is raised up, turning on mirror transistor *M*2 and changing the output voltage.

The voltage drop across the transistor M1 causes the gate-source voltage of the off transistors in the PUN to become positive, yielding an exponential reduction in sub threshold leakage due to the phenomenon called the stacking effect. It should be noted that if the body effect is not eliminated due to the unequal voltage of the source and body terminals, the leakage current will be decreased further at the expense of higher deviation due to process variations. The voltage across the diode footer in other domino circuits that use a diode-footed techniques such as DFD and CKCCD must be decreased to zero in order to lower the dynamic node voltage to zero. But in the proposed circuit, it is not necessary for this voltage to reach 0 V since the current of the diode footer is needed instead of the voltage across it. Therefore, the size of the diode-footer transistor *M*1 in the proposed circuit is smaller than other DFD circuits. Consequently, a lower leakage current must be compensated by the keeper transistors instead of the larger one in the other circuit due to the larger size of the footer and mirror transistors.

This results in lower delay and power consumption and area overhead. On the other hand, in the next pre discharge mode, the dynamic node is charged from nonzero voltage to power supply voltage, yielding reduction in the power consumption with respect to the existence of the large capacitance on the dynamic node in wide fan-in gates, especially wide fan-in OR gates. In addition, since transistor *M*1 increases the switching threshold voltage of the PMOS transistors, the new switching threshold voltage of the gate is about twice the threshold voltage of the PMOS devices. [1]

3. CLAMPED BITLINE CURRENT SENSING AMPLIFIER

A commonly used current mode sensing amplifier is the clamped bit-line sense amplifier By clamping the voltage on the bit-line with a stable voltage (VREF) the signal current produced by the cell can be transferred to an internal sense amp node without charging/discharging the large bit-line capacitance. As a result, both sensing delay and dynamic power consumption are significantly decreased. [8]

The sense amplifier as shown in figure 3 uses three pre-charge and equalization transistors (M7, M8 and M9), two current sensing transistors (M5 and M6) and four back to back inverter configuration transistors for the voltage output stage (M1, M2, M3, M4). Its operation follows two stage pre-charge/equalization, and sensing. The following is the timing schedule:1) transistors M7, M8, M9 are turned on to pre-charge and equalize the sensing nodes, 2) transistors M7 and M8 are turned off and the memory cell accessed, 3) the current from the cell starts being sourced by one of the transistors M1 and M2 and a voltage difference starts forming on one of the output nodes, 4) this voltage is further amplified by the positive feedback amplifier until it reaches the latched state.It has been shown that the time response of a latch formed by cross-coupled inverters is directly related to the AC small signal gain bandwidth (GBW) product of the inverters. Maximizing GBW product maximizes the speed of the sense amplifier.

Table 1. Comparison of Parameters

PARAMETERS/ TECHNIQUES	Power (Watts)	Area (m^2)	Delay (Sec)	Leakage Power (Sec)
CCD	1.7873 X 10^{-3}	836 µm^2	2.681 X 10^{-8}	3.6107 X 10^{-9}
CBLSA based CCD	1.0231X 10^{-4}	836 µm^2	4 X 10^{-9}	2.748 X10^{-11}

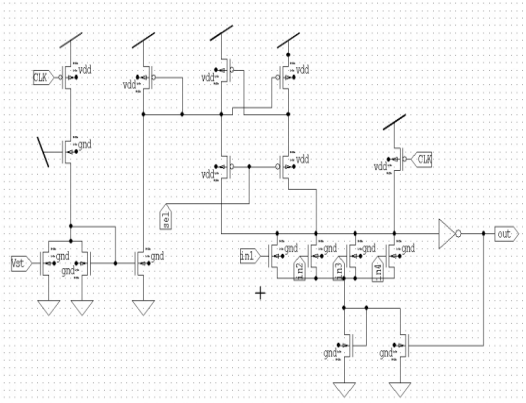

Figure 3 CCD uses Clamped bit-line Current-sensing Amplifier

By examining both small signal models for the positive feedback, cross-coupled voltage sense amplifier and the clamped bit-line current sensing amplifier we can derive the following GWBs:(a) voltage sensing and (b) current sensing GWB Since $C_d << C_{BL}$ it can be easily seen that the current mode sense amplifier enjoys a much higher speed. Another observation is that this amplifier is bit-line capacitance insensitive maintaining a constant speed over increased bit-line capacitance. To recognize the power savings associated with the switch to current sensing amplifiers we need to examine the dynamic power dissipation of the voltage sensing amplifier. In voltage sensing, the bit-line is discharged and charged by dVBL (close to 400mV) for every read operation. When this dVBL is combined with both increasingly large bit-line capacitance CBL, and read frequency "fread" the energy following the below equation becomes large. The current sensing amplifier on the other hand has a very negligible voltage swing, thus nearly eliminating dynamic power dissipation. As a result, both sensing delay and dynamic power consumption are significantly decreased. Furthermore, this bit-line voltage inactivity significantly decreases cross talk between bit-lines, and supply voltage drop associated with bit-line charge up.

4. RESULTS AND DISCUSSION

In this proposed work, we have introduced Clamped bit line current sensing amplifier with CCD and the parameters like power, area, delay, power delay and leakage power is compared as shown in table 1. Power consumption and delay has been reduced with clamped bit line current sensing amplifier since power plays a vital role in VLSI. The area is found to be the same in existing and proposed work.

5. CONCLUSION

In older technique, CCD increased power consumption with high leakage current. The most commonly used Clamped bit-line current sensing amplifier shows a large increase in speed and significant decrease in power consumption. In addition, the current sensing amplifier provides a bit-line-capacitance-independent performance, which is crucial to future memory capacity increases. By eliminating voltage changes on the bit-line the current sense amplifier also eliminates cross talk and voltage supply bounce. Simulation results using Tanner confirmed considerable development in leakage reduction and suitable speed for high-speed applications.

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