Design of CMOS based Transimpedance Amplifier for Bandwidth Enhancement with Large Gain

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ABSTRACT
This paper present a differential architecture of cmos transimpedance amplifier is offered to obtained the input capacitive load in-sensitive and the very minimum noise structure. The suggested TIA is dependent on the differential structure and composed of a regulated cascode block and a differential amplifier along with active feedback. To increase the bandwidth of the amplifier series inductive peaking and a capacitive degeneration step employed. Simulation results shows that the TIA achieves 100 GHz bandwidth, 80.4 dBΩ transimpedance gain, and 20 pA/ $\sqrt{Hz}$ of the input referred noise current, and it dissipates 10 mW under 1.2V supply. Theproposed TIA increases the bandwidth by more than two times when compared with other existing CMOS TIAs, while achieving comparable performance in other performance metrics.

Keywords
CMOS, Inductive series peaking, Transimpedance amplifier (TIA), Bandwidth enhancement, RGC, Capacitive degeneration, Active feedback.

1. INTRODUCTION
One of the communication type called as Fiber-optic has been migrated from the telephony to the wide-area-network architecture in which the low attenuation provides the large distances and bandwidth of the silica-fibers to keep the high capacity for information to the less range like the memory links, storage-area networks or for the chip-scale signals that are global in which the requirements of processing needs the bandwidth which is not obtained over the electrical inter-connections [1], Emerging networks of telecommunication and the data-communication techniques has increase the attention in the high speed of the optical or the electronic devices of the network. The IEEE-802.3ba standard supports 100 Gb/s optical communications.[17]. Broadband receivers are required for high-speed optoelectronic (O/E) signal conversion. Conventionally, broadband electronics adopt III-V semiconductor technologies such as GaAs and InP [4]. Modern optical receiver design places a high premium on speed and energy efficiency and receiver design metrics focus on the transimpedance gain-bandwidth versus the power consumption.[4] A standard optical receiver normally contains of a transimpedance amplifier (TIA), a limiting amplifier (LA), a clock, data recovery block, and a digital signal processor. The photodiode of a receiver transforms the light intensity to a current signal. Then the TIA converts the current signal into a voltage signal, while amplifying the signal.[17]. CMOS is considered as the best candidate for the complete integrated design of TIA because of their cost, their integration in the system and its manufacturing have the ability that is beneficial and also provide the reliable speed and performances of the noise simultaneously [2]. At high-frequency, the overall receiver bandwidth is typically limited by the photodiode capacitance , the input TIA capacitance , along with input resistance value of transimpedance step.[4] In order to collect the optical energy that is enough for the huge area photo-diode is acceptable that provides the huge range of capacitance. Various CMOS-TIA framework may have also been explained that the representing the various input phases for differentiating higher values of the input-capacitance of photo-diode for efficient bandwidth examination, like the common-gate (CG), the input-stage CG feed-forward is one of the topology which is having the negative feed-back [17]. The regulated-cascode (RGC) input-stage is the fundamentally a common gate configuration with active feedback to deliver lower input impedance than simple common gate input stage does. Therefore, better separation of the relatively large input parasitic capacitance from the bandwidth estimation may be obtained [3]. Capacitive degeneration or peaking, uses the capacitive components to add the one zero extra which adjust the dominant-pole or the extra-pole to apply the well-monitored response in the system. In this also the inductive peaking is proved to be an efficient method in both reduction of noise and improvement of the bandwidth [7]. Shunt inductive peaking [8], [9] simply uses inductor in series with the load resistor to maintain a constant effective load over a higher frequency range. Series inductive peaking [10], [11] normally employs inductors between active devices of gain stages or between active device and capacitive load at input/output node so that the collective parasitic capacitances at each node are split into LC networks. This paper presents a TIA topology to balance the huge range of capacitance may be achieved through the photo-diode which is also obtained through the minimum value of input impedance as compare to the simple common-gate at the input stage. And this type of input-stage is dependent on the cross-coupled current-conveyor architecture [16]. The proposed TIA relaxes the bandwidth limitation at the input node and shows a stable performance over a wide-ranging capacitive load. This differential TIA structure with inductive peeking and capacitive degeneration stages also brings a huge improvement in noise performance as the single-ended input-referred noise current of the overall circuitry is measured to be below 10 pA/$\sqrt{Hz}$ In Section II, the detailed designing of circuit and detailed determination of suggested method of TIA is described; with in the Section-III, the results of simulation suggested the structure which is described in this section. At the end, within the Section-IV, the conclusion is given along with all the possible enhancement for the future.

2. DESIGN OF PROPOSED TIA

2.1 Schematic of Proposed TIA

The primary objective of the proposed TIA is that a minimum bandwidth of 100 GHz and other objectives of the TIA includes high transimpedance gain and low input referred noise. Differential signaling protects signals from external noise aggressors and reduces supply noise coupling to minimal, which can be highly useful for TIA design due to its very low input signal level.

The proposed TIA shown in Fig. 1 consists of a RGC block followed by a differential amplifier with a negative feedback block. It is considered that differential photodiode current sensing for the input of the TIA. The receiving photo-diode is a current source In with parasitic capacitance Cpd. The photodiode current is converted to a differential signal by the biasing circuit shown in Fig. 1 [5]. Two capacitors, CB1 and CB2, block the DC voltage, therefore isolating the DC bias voltage of photodiode from RGC input stage. The photodiode is reverse biased with resistors RB1 and RB2 and the supply voltage The input current of a photo diode is small, in the order of micro-amperes, which necessitates low input impedance for the RGC block. Each RGC circuit is a common gate (CG) amplifier with a local feedback. The local feedback formed by M2 and R2 for the upper RGC circuit is a common source amplifier, which generates a negative feedback voltage at the gate of M1. The feedback increases the effective transconductance (gm) of common gate amplifier is to reduce the input resistance [1]. Reduction of the input resistance also isolates the input pole associated with the large parasitic capacitance Cpd. It reduces the impact on the TIA bandwidth to result in an improved frequency response. The second stage of the proposed TIA consists of a capacitive degenerate differential amplifier M5/M6 with a negative feedback network formed by M7/M8. The stage intends for a bandwidth compensation in order to increase the gain-bandwidth product. The capacitive degeneration introduces a high-frequency peaking zero to the system, and the feedback network further increases the bandwidth by a factor of (1 + loop-gain). The differential stage combined with the RGC block performs a stagger tuning for the frequency response, compensating the pole in one stage with the peaking in the following stage as elaborated in the following.

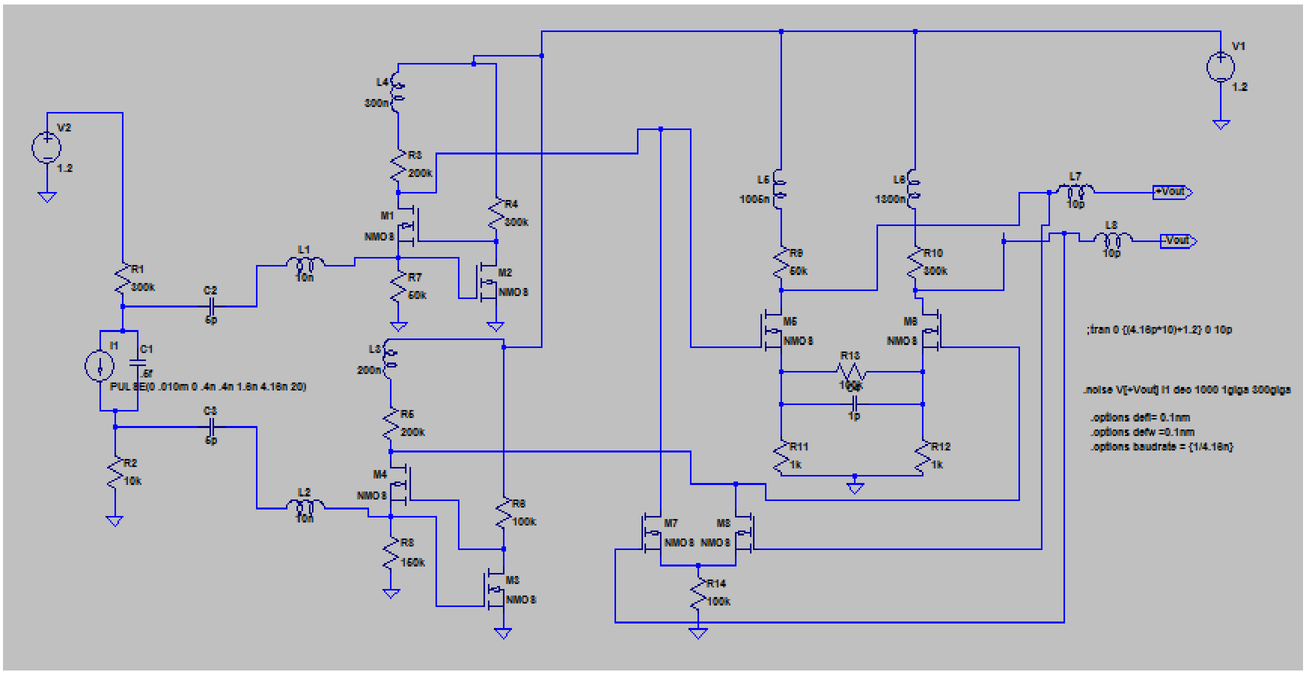

Fig 1: Circuit of proposed TIA

2.2 RGC Stage

The RGC input stage in fig. 1(a) is well suited for broad-band TIA design by its very low input impedance, which could be resulting from small signal circuit model in fig.2. where, $C_i \approx C_{sb1} + C_{gs2}$ and $C_j \approx C_{gs1} + C_{gd2}$. The small signal input resistance is therefore given by

$$r_i = Z_{in}(0) \approx \frac{1}{g_m(1+g_{m2}R_2)} \qquad (1)$$

This is one of the small input that impedance in the maximum part which also separate the capacitance of photo-diode from the bandwidth and hence, not similar to the common-gate or the common resource of TIAs, then the dominant-pole of the RGC TIA is normally placed in the amplifier other than the input-node as mentioned [9].

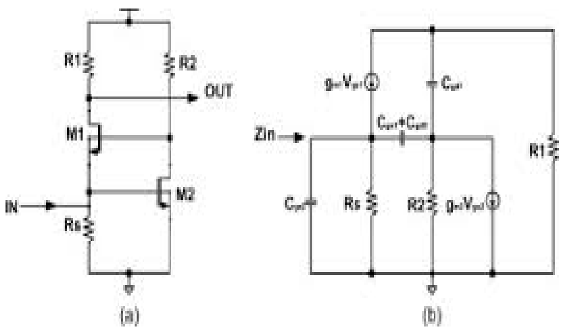

Fig 2: RGC stage. (a) Circuit schematic. (b) Small- Signal model

2.3 Capacitive Degeneration Stage

The capacitive degeneration network formed by R_S and C_S introduces an additional peaking in the frequency response. Considering it as a simple common source amplifier, the location of the zero is obtained as

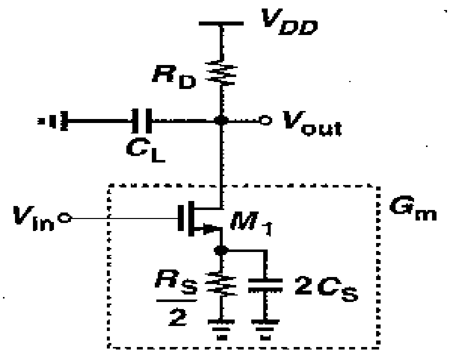

Fig 3: Capacitive Degeneration Stage

The voltage gain of a gain stage with capacitive degeneration is expressed by

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m1}\ R_1}{1 + g_{m1}R_s}\frac{1 + sR_sC_s}{1 + s\dfrac{R_sC_s}{1 + g_{m1}R_s}} \qquad (2)$$

which contributes a zero at $\frac{1}{R_sC_s}$ and a pole at

$(1+ g_{m1}R_s) /R_s\ C_s$. The zero could be used to recompense the leading pole of circuit. And -3 dB cut-off of the frequency is then achieved through another circuit's lowest pole.

2.4 Series Inductive Peaking

Series peaking L1 inductor are adopted for the proposed TIA to increase the BWER by reducing the capacitive loading effect of the photodiode [8].

Here three broad- band design techniques introduced in section II are combined together to design a high performance TIA in this section. RGC input stage consist of two NMOS transistor M1 and M2 provide low input impedance in TIA.

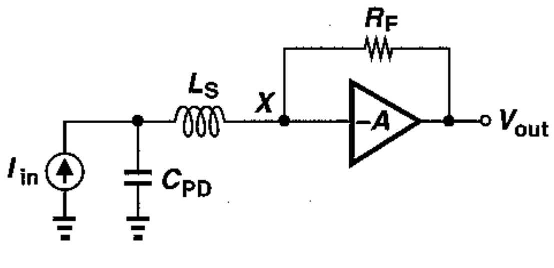

Fig 4: Series Inductive Peaking

Inductive series peaking in the circuit employed by using inductor L1 provides peaking effect and enhances the bandwidth [12]. Two stages of capacitive degeneration employed by using NMOS M3 and M4 enhances the overall bandwidth and TIA is capable to operate in high frequency ranges. Also this design is capable to reduce the equivalent input noise current below a certain limit [14].

$$\frac{V_{out}}{V_{in}} = \frac{-1}{S^2+\frac{R_F}{(A+1)L_S}S+\frac{1}{C_{PD}\,L_s}}\frac{AR_F}{(A+1)C_{PD}\,L_S} \qquad (3)$$

$$\omega_{-3dB} \approx \frac{\sqrt{2}\,A}{R_F C_{PD}} \qquad (4)$$

2.5 Noise Analysis

The corresponding input noise current, also called input-referred noise current, is a significant figure of merit of TIAs in that it directly affects the optical link budget. Bit error rate (BER) of an optical front-end can be expressed in terms of the total corresponding input noise current $i_{total\,,n,eq}$ by

$$BER = Q\left(\frac{i_{in,pp}}{2i_{total\,,n,eq}}\right) \qquad (5)$$

Where, $i_{in,pp}$, is the peak to peak input current signal amplitude and $Q(x) = \int_x^\infty (\frac{1}{\sqrt{2\pi}})$ exp(-(x^2 /2)) dx. The corresponding input noise current is defined in such a way that together with a noiseless TIA, it reproduces the same output noise as the actually noisy TIA. Although the TIA noise model can be conveniently represented by a noise current source only, the equivalent input noise current is dependent on the source impedance, which is mainly determined by the photodiode capacitance and the matching network [6].

3. SIMULATION RESULTS

TIA in this section. RGC input stage consist of two NMOS transistor M1 and M2 provide low input impedance in TIA.

Inductive series peaking in the circuit employed by using inductor L1 provides peaking effect and enhances the bandwidth [12]. Two stages of capacitive degeneration employed by using NMOS M3 and M4 enhances the overall bandwidth and TIA is capable to operate in high frequencyranges. Also this design is capable to reduce the equivalent input noise current below a certain limit [14].

The input current of a photo diode is small, in the order of micro-amperes, which necessitates low input impedance for the RGC block. RGC circuit is a common gate amplifier with a local feedback [5]. The local feedback formed by M1 and R3 for the upper RGC circuit is a common source amplifier, which generates a negative feedback voltage at the gate of M2. The feedback increases the effective transconductance (gm) of the common gate amplifier to reduce the input resistance [10]. And then reduction of input-resistance may also separate down the input-pole that are related with huge parasitic-capacitance i.e. Cpd. It reduces the impact on the TIA bandwidth to result in

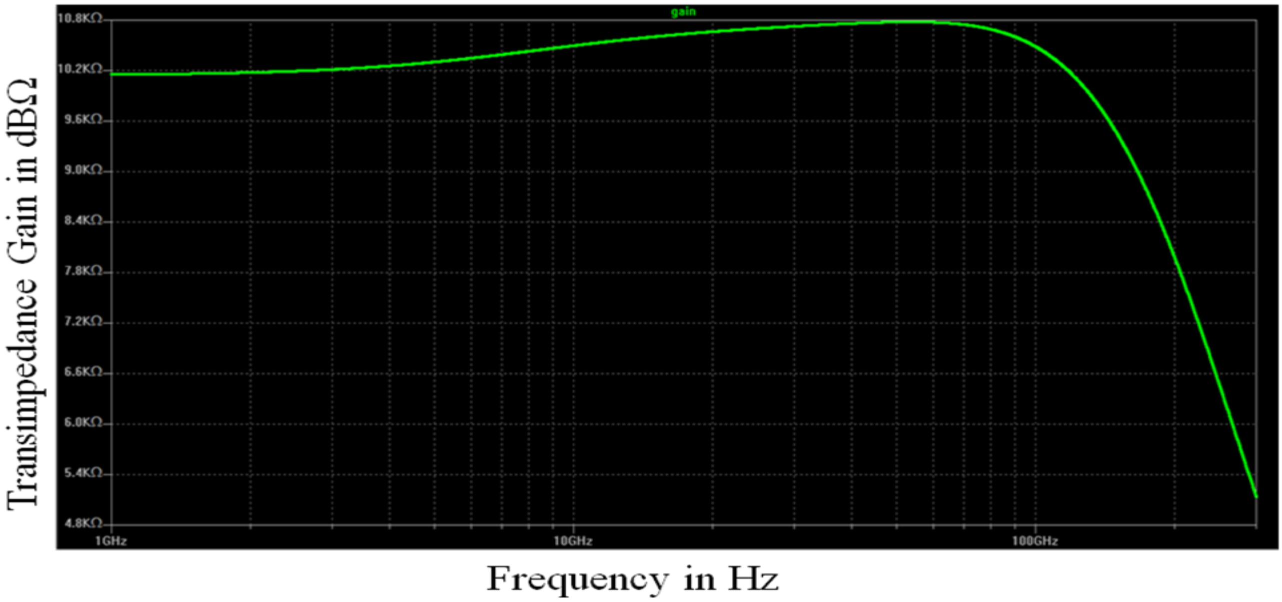

Fig 5: Impact of Capacitive Degeneration and inductive Peaking

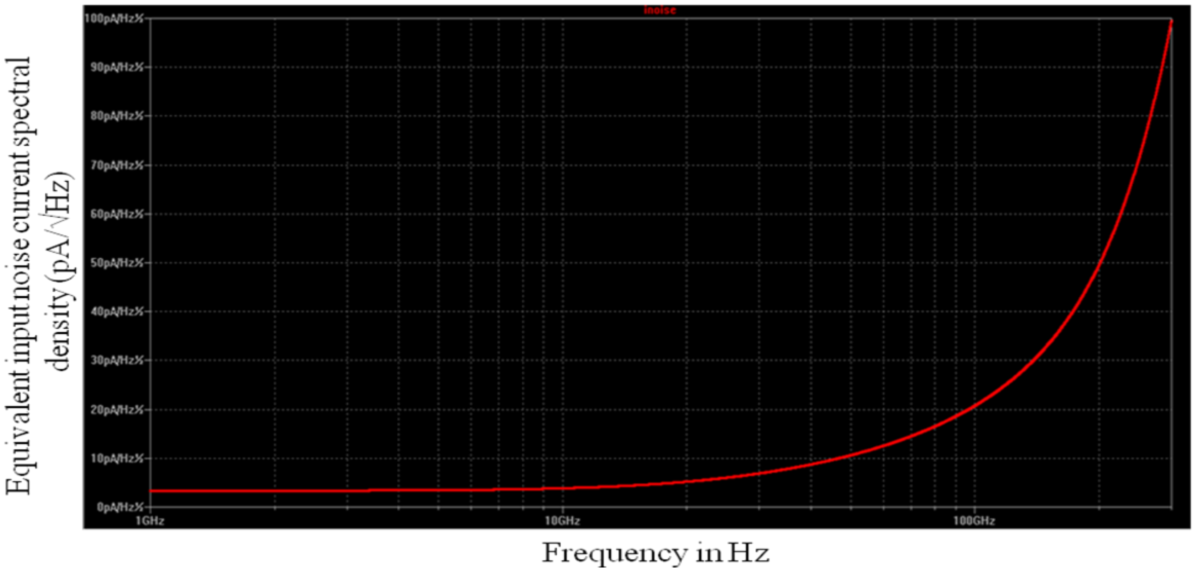

Fig 6: Simulation of Equivalent input noise current spectral density

an improved frequency response. The second stage of the proposed TIA consists of a capacitive degenerate M3 and M4. The stage intends for bandwidth compensation in order to increase the gain-bandwidth product. The capacitive degeneration introduces a high-frequency peaking zero to the system, and the feedback network further increases the bandwidth by a factor of (1 + loop-gain) [11].

In fig.5 simulation of transimpedance gain is observed by employed series inductor. -3db gain of TIA with series inductor is 80.4 dBΩ at frequency 100 GHz. So by apply series inductor bandwidth of TIA can be increased.

In fig. 6 shows the simulation of input noise current spectral density it can be observed 20.8 pA/$\sqrt{Hz}$.

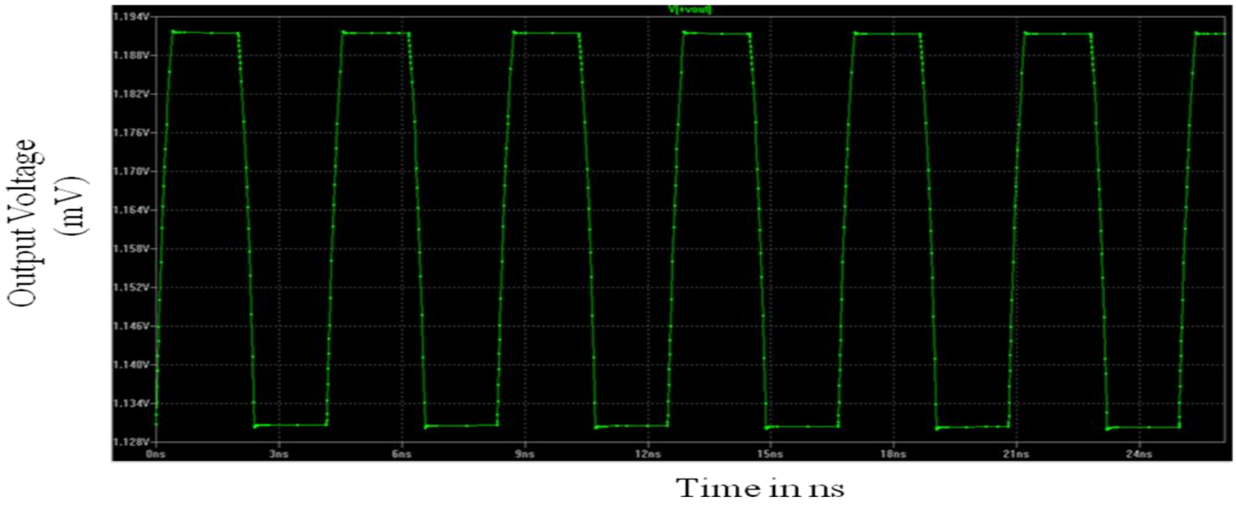

Fig 7: Simulation of output voltage

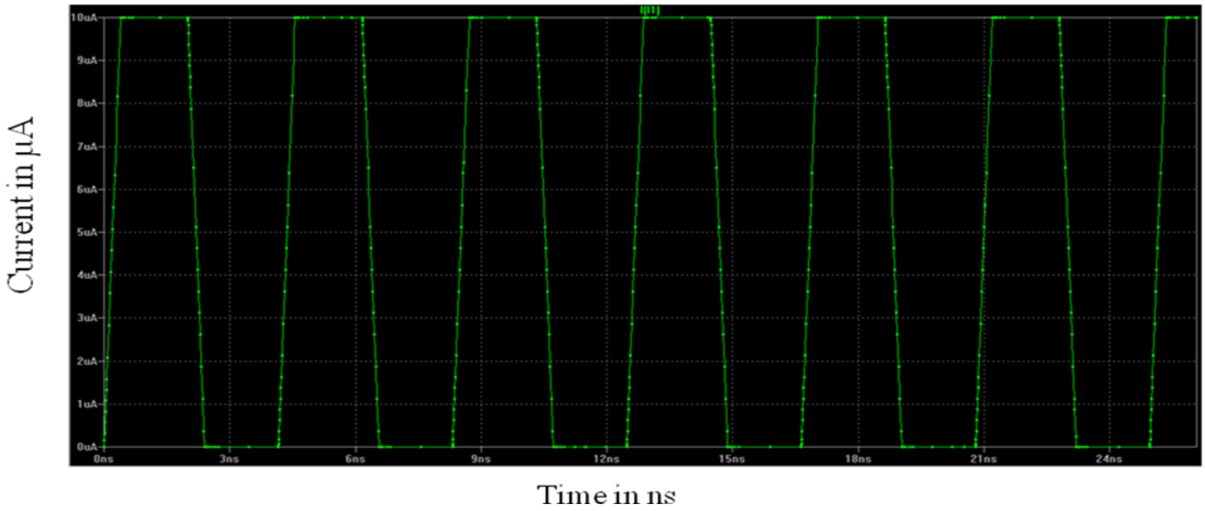

Fig8: Simulation of input current

In Fig.7 Simulation result shows the amplified output voltage observed 1.19 V in response to 10µA input current.

Fig. 8 shows the simulation of input current which is equivalent to photodiode output current.

Table 1. Performance Comparison of CMOS TIAs

Reference	Supply	Gain (dbΩ)	Bandwidth (GHz)	Noise (pA/$\sqrt{Hz}$)	Power Dissipation (mW)
[1]	1.2	46.7	21.6	30	39.9
[2]	1.2	54	41	11	168
[3]	1	55	31	23	9
[4]	1.2	40	70	31	24
This work	1.2	80.4	100	20	10

4. CONCLUSION

A bandwidth enhancement method for broad-band TIA design is proposed, which is based on a exclusive combination of series inductive, capacitive degeneration, RGC input stage.

Simulation results of transimpedance gain is 80.4 dBΩ. The simulated value of input referred noise current is 20 pA/$\sqrt{Hz}$.

5. REFERENCES

[1] S. Bashiri, C. Plett, J. Aguirre and P. Schvan “A 40 Gb/s transimpedance amplifier in 65 nm CMOS,” International Symposium on Circuits and Systems (ISCAS), pp. 757-760, May 2010.

[2] S. T. Chou, S. H. Huang, Z. H. Hong, and W. Z. Chen “A 40 Gbps optical receiver analog front-end in 65 nm CMOS,” International Symposium on Circuits and Systems (ISCAS), pp 1736-1739, May 2012.

[3] J. Kim and J. F. Buckwalter, “Bandwidth enhancement with low groupdelay variation for a 40-Gb/s transimpedance amplifier,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 1964-1972, August 2010..

[4] Maruf N. Ahmed, Joseph Chong, and Dong Sam Ha “ A 100 GB/s Transimpedance Amplifier in 65 nm CMOS Technology for Optical Communications” Multifunctional Integrated Circuits and Systems..

[5] Dandan Chen, Kiat Seng Yeo, Senior Member, IEEE, Xiaomeng Shi, Manh Anh Do, Senior Member, IEEE Chirn Chye Boon Senior Member, IEEE, and Wei Meng Lim, “Cross-Coupled Current Conveyor Based CMOS Transimpedance Amplifier for Broadband Data Transmission” IEEE transactions on very large scale integration (vlsi) systems, vol. 21, no. 8, august 2013.

[6] H. Ikeda, T. Ohshima, M. Tsunotani, and T. K. T. Ichinoka, “An auto gain control transimpedance amplifier with low noise and wide input dynamic range for 10-Gb/s optical communication systems,” IEEE J. Solid-State Circuits, vol. 36, no. 9, pp. 1303–1308, Sep. 2001.

[7] B. Analui and A. Hajimiri, “Bandwidth enhancement for transimpedance amplifiers,” IEEE J. Solid-State Circuits, vol. 39, no. 8, pp. 1263–1270, Aug. 2004.Y.T. Yu, M.F. Lau, "A comparison of MC/DC, MUMCUT and several other coverage criteria for logical decisions", Journal of Systems and Software, 2005, in press.

[8] H. H. Kim, S. Chandrasekhar, C. A. J. Burrus, and J. Bauman, “A Si BiCMOS transimpedance amplifier for 10-Gb/s SONET receiver,” IEEE J. Solid-State Circuits, vol. 36, no. 5, pp. 769–776, May 2001.

[9] B. Razavi, Design of Integrated Circuits for Optical Communications. New York: McGraw-Hill, 2003.Y.T. Yu, M.F. Lau, "A comparison of MC/DC, MUMCUT and several other coverage criteria for logical decisions", Journal of Systems and Software, 2005, in press.

[10] F. Yuan, “Low-voltage CMOS current-mode preamplifier: Analysis and F. Yuan, “Low-voltage CMOS current-mode preamplifier: Analysis and 26–39, Jan. 2006.Spector, A. Z. 1989. Achieving application requirements. In Distributed Systems, S. Mullender

[11] E. Sackinger, “The transimpedance limit,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 1848–1856, Aug. 2010.

[12] F. Tavernier and M. S. J. Steyaert, “High-speed optical receivers with integrated photodiode in 130 nm CMOS,” IEEE J. Solid-State Circuits, vol. 44, no. 10, pp. 2856–2867, Oct. 2009.

[13] S. Goswami, T. Copani, B. Vermeire, and H. Barnaby, “BW extension in shunt feedback transimpedance amplifier using negative miller capacitance”, in Proc. IEEE Int. Symp. Circuit Syst., Jun. 2008, pp. 61–64.

[14] W. Z. Chen and C. H. Lu, “Design and anaylsis of a 2.5-Gb/s optical receiver analog front-end in a 0.35-μm digital CMOS technology,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 53, no. 5, pp. 977–983, May 2006.

[15] Omeed Momeni, Student Member, IEEE, Hossein Hashemi, Member, IEEE, and Ehsan Afshari, Member, IEEE A 10-Gb/s Inductorless Transimpedance Amplifier IEEE transactions on circuits and systems—II: express briefs, vol. 57, no. 12, december 2010

[16] S. T. Chou, S. H. Huang, Z. H. Hong, and W. Z. Chen “A 40 Gbps optical receiver analog front-end in 65 nm CMOS,” International Symposium on Circuits and Systems (ISCAS), pp. 1736-1739, May 2012.

[17] Zhenghao Lu, Kiat Seng Yeo, Wei Meng Lim, Manh Anh Do, Senior Member, IEEE, and Chirn Chye Boon, “Design of a CMOS Broadband Transimpedance Amplifier With Active Feedback” IEEE transactions on very large scale integration (vlsi) systems, vol. 18, no. 3, march 2010.