A Survey Paper on Implementing MTCMOS Technique in Full Subtractor Circuit

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ABSTRACT
This paper presents the study and survey analysis of Full Subtractor circuit on implementing the MTCMOS technique. Full Subtractor is a combinational circuit that performs subtraction and results in difference and borrows outputs. Implementing the MTCMOS technique on this circuit results in reduction of both leakage current and power consumption.

Keywords
Full Subtractor, MTCMOS, leakage current, power dissipation.

1. INTRODUCTION
In recent years, the usage of portable devices such as laptops, Smartphone, computers has been increased to great extent .The recognition and need of these portable electronic devices compels designers to aim for small silicon area, advanced speed , low power consumption and reliability. But these parameters are major concern in schematic design before their actual implementation in the layout. Thus minimum number of transistors should be used to consume limited area and power. In all digital circuits, arithmetic circuits play an important role. Subtractor is one of most significant and critical components of them. There are various possible logic styles compared to the basic CMOS logic style. Thus we focus on area and power efficient design of subtractor to design small portable devices .Low power VLSI design can be classified into two major categories: Analysis and Optimization. Both business and technical field interest in driven of low power chips and systems. With rapid expanding market, demand for low power electronic products is booming. Due to increased device density, speed and complexity semiconductor industries present rigorous requirements to power distribution of digital chips.

2. SUBTRACTOR
A subtractor is one of the four basic binary operations, which performs the subtraction. Subtractors are not only applied on arithmetic calculations, but in other parts of processor. It operates on binary numbers and results in binary numbers. Depending upon the purpose of the application to be performed, inputs vary. For two inputs, half subtractor is used and if we have three input we apply full subtractor to get the outputs.

2.1. Full Subtractor
A Full subtractor is a combinational circuit that performs a subtraction between two binary bits and can borrow 1 from lower significant stage. Thus circuit has three inputs and two outputs. Let A,B and Borrow in (Bin) be three inputs and two outputs Borrow out (bout) and Difference (Diff).It can be design by two 2-input EXOR gate, two 2-input AND gate, two 1-input inverter and single 2-input OR gate. The gate level of Full Subtractor has been shown in Figure 1 and Truth table 1.Booleanexpressions for the two output variables are obtained from karnaugh map.

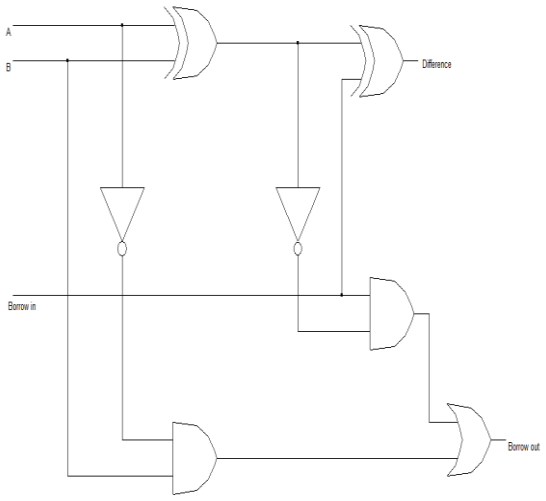

Figure 1. Gate-level Full Subtractor

Table 1. Truth table of Full Subtractor

A	B	Borrow in (Bin)	Borrow out (Bout)	Difference (Diff)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Boolean expressions are –

1. Difference $=A \oplus B \oplus B_{in}$

$=AB\ B_{in} + A'B'\ B_{in} + A'B\ B_{in}' + AB'\ B_{in}'$

2. Borrow $= A'B + A'\ B_{in} + B\ B_{in}$

$=AB\ B_{in} + A'B'\ B_{in} + A'B$

3. DIFFERENT PARAMETERS
The performance assessment of full subtractor is established on area and power consumption, power delay, power dissipation and Power-Delay-Product. Area, speed and power consumption are the main issues in VLSI design which conflict with each other and act as constrain on the design of VLSI circuits. On the basis of different logic styles, various designs of full subtractor are individually investigated, analyzed on these performance criteria.

3.1 Power Parameter calculation

Due to lower power dissipation in Complementary Metal-Oxide Semiconductor (CMOS), it has advantage over other completing technologies like Transistor- Transistor Logic (TTL) and Emitter Coupled Logic (ECL). Multiple Threshold CMOS (MTCMOS) isolates low threshold circuits from power and ground support using high threshold devices. Power dissipation is approximately proportional to the square of voltage supply. Thus lowering the supply voltage is the most competent way to achieve low power performance. To maintain the switching speeds of high transistors we need to scale down the threshold voltage. But this causes the significant amount of leakage power dissipation even when the transistor is not switching.

The main parameters that contribute to the total power dissipation are dynamic power, static power and short-circuit power. The expression can be stated as below-

$T_{total} = P_{dynamic} + P_{static} + P_{short\text{-}circuit}$

3.1.1 Dynamic Power Dissipation

It attributes mainly in the power dissipation. Due to capacitive charging and discharging of the output wiring and when transistor switches state from ON to OFF and vice versa, causes the dynamic power dissipation. Short circuit current is produced when there is no load capacitance. With the hike in capacitive load, charge and discharge current starts prevailing the main current.

$P_{dynamic} = K.C.V^2_{dd}.F_{sw}$

Where,

K = Technology factor

C = Capacitance of switching nodes

V_{dd} = Supply voltage

F_{sw} = Effective switching frequency

The equation of dynamic power dissipation can be constructed with the assumption that rise time and fall time of the step input is much less than the repetition period. The above equation represents that the average dissipated power is proportional to energy required to charge and discharge the capacitance load.

3.1.2 Short Circuit Power Dissipation

Short circuit power is part of dynamic power consumption, it relied on signal transition. It occurs due to rise time and fall time of signal. For short period of time PMOS and NMOS are ON, so there will be a path from V_{dd} to V_{ss}. Therefore it is factor of supply voltage and directly proportional to V_{dd}. With the reduction in V_{dd}, t_r and t_f parameters will increase.

$P_{sc} = I_{sc}. V_{dd}. t_s. f_{sw}$

Where,

f_{sw} = Switching frequency

I_{sc} = Short circuit current

t_s = Switching delay

V_{dd} = Supply voltage

3.1.3 Static Power Dissipation

The static power dissipation is the product of leakage current and supply voltage. The total static power dissipation P_s is given by

$P_s = \sum_l^n$ Leakage current×Supply voltage

Where,

n = Number of devices

3.2 Leakage Current Calculation

The leakage current equation can be represent as

$i_o = i_s (e^{qV/kT} - 1)$

Where,

i_s = Reverse saturation current

V = Voltage of diode

q = Electronic charge

k = Boltzmann constant

T = Temperature

Sub threshold or weak inversion conduction current between source and drain in a MOS transistor occurs when gate voltage is below the transistor threshold voltage. The Sub threshold or weak inversion current I_{ds} can be written as-

$I_{ds} = I_{dso} e^{(Vgs - Vt / nVT)} [1- e^{Vds/VT}]$

$I_{dso} = \mu_{eff} c_{ox} (W/L) V_T^2$

Where,

μ_{eff} = Charge carrier mobility

c_{ox} = Gate capacitance / unit area

W/L = Width to length ratio of channel

V_t = Threshold voltage

V_T = Thermal voltage

n = Sub- threshold swing coefficient

V_{gs} = Gate to source voltage

V_{ds} = Drain to source voltage

4. TRANSISTOR GATING

In this technique two sleep transistor PMOS and NMOS are inserted in between supply voltage and ground. A PMOS is implanted in between pull-up network and network output. A NMOS is inserted in between pull down network and ground. During standby mode both sleep transistor are turned off. To reduce the voltage in power supply, method requires to reduce transistor threshold voltage to maintain noise margins and output. But this increases the sub threshold leakage current in p and n MOSFET's, increasing the overall power consumption. Thus transistor gating technique is implemented to reduce the power dissipation and leakage current. MTCMOS (Multi Threshold CMOS) technique has two main features:

(1) Two operational modes, active and sleep mode to organize the power management.

(2) Two dissimilar threshold voltages cutting off the low V_t from power supply and high V_t from ground circuit.

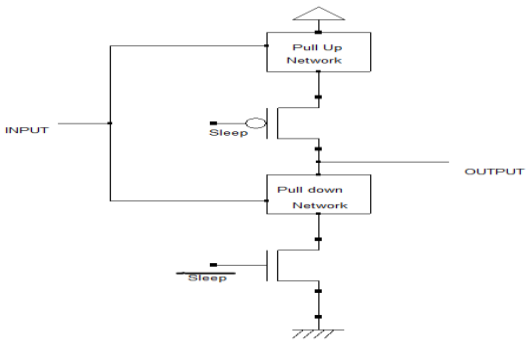

Figure 2. Transistor Gating Technique

5. LITERATURE SURVEY

[1] In 2012, Milind Gautam, Shyam Akashe proposed Transistor Gating technique implemented in Full subtractor circuit. In this paper, low-power design techniques proposed to minimize the standby leakage power in nanoscale CMOS. The tool used for schematic simulation is CADENCE VIRTUOSO in 45 nm technology. This technique results in reduction in leakage current by 17.58% and 24.38% reduction in leakage power.

[2] In 2015, Dr.PR Reddy, Dr. KV Ramanaiah, MM Basha presented different design circuit on full Subtractor implanting the MTCMOS technique. The tool used is Microwind 3/DSCH in 65nm technology. The BSIM 4 parameter analyzer is used to analyze the proposed circuit. The proposed design of 14 transistor 1-bit Full subtractor at 1.0 v results in power consumption of 1.896 µw, I_{ddmax} is 0.197 mA , area as 240 μm^2 and delay power calculated is 131ps.

[3] In 2013, a paper presented by M. Gautam and S. Akashe on a full subtractor using MTCMOS technique to minimize the active leakage power. Simulation result is done at 0.7 volt designing on CADENCE VIRTUOSO tool in 45 nanometer technology. The proposed design results in reduction of leakage current by 15.63% and power is 95% compare to conventional full subtractor circuit.

[4] In 2015, S. Krishna, Raghu MC and S. Faris propose a paper intended to minimize leakage power and circuit area. The results were carried out in LT Spice and Microwind/DSCH software. Layout area required is 633.1 μm^2 and noise power calculated as 33.89 pV.

Table 2. Literature Survey Table

S. No	Journal	Topic	Technology	Parameter	
				Power consumption (Reduction %)	**Leakage current (Reduction %)**
[1]	IEEE (2013)	Transistor gating: reduction of leakage current and power in full subtractor circuit.	Cadence Virtuoso in 45 nm	4.081×10^{-3} watt in 0.7v (24.38%)	280.2pA (17.58%)
[2]	IEEE (2015)	Novel energy efficient 1-bit full subtractor at 65nm technology	Microwind / DSCH in 65nm	1.896 µwatt in 1.0 v	$I_{dd\ max}$ =0.917 mA I_{ddavg}= 0.002 mA
[3]	IEEE (2013)	Reduction of leakage current and power in full subtractor using MTCMOS technique	Cadence Virtuoso in 45nm	1.4508µwatt in 0.7 v (95%)	228.65 fA (15.63%)
[4]	IJARECE (2015)	An efficient design of full subtractor cell and its application in ripple borrow subtractor	Microwind / DSCH 2, LT Spice in 35 nm	2.65 milli watt in 0.7 v	-
[5]	IJRECE (2014)	Reduction of leakage current and power in full subtractor using MTCMOS technique	LT Spice in 16 nm	(98%)	Active mode =0.528 µA Standby mode =1.95 pA in 0.9v (45%)
[6]	IJSR (2014)	Power reduction approach in combinational circuit	Tanner S-edit 13.0 in .25 µm	23 milli watt in 5v (78%)	3.2µA
[7]	IJESR (2014)	Static power dissipation reduction on full subtractor using MTCMOS	Tanner S-edit T-Spice in TSMC018	1.199×10^{-8} watt in 0.7v (81%)	-

[5] In 2014, MD Saroja and MR Naik proposed a paper to reduce the leakage current on implementing MTCMOS approach in full subtractor circuit. Reduction in current is almost 90% in 16nm technology. Simulation result is executed at 0.9 volt for schematic and LT Spice for simulation in 45nm, 32nm, 28nm and 16nm technology.

[6] In 2014, N. Rawat and R. Jain recommended a paper on power reduction approach in combinational circuit. MTCMOS way is implemented in which drain gating technique is used in proposed full subtractor circuit. The software for simulation used is Tanner S-edit 13.0.

[7] In 2014, k. Spandana and K. Sujitha proposed static power dissipation on full subtractor using MTCMOS technique. In this power gating is applied in full subtractor circuit using different leakage power reduction techniques like MTCMOS, Variable Body – Bias. The design software is Tanner S-edit and simulated under T- Spice tool in TSMC018 technology.

6. CONCLUSION

This survey paper analysis of Full Subtractor circuit can be concluded that reduction in power dissipation and leakage current is possible to great extent, on implementing the techniques like transistor gating, power gating and drain gating. In future, varying the W/L ratio in sleepy transistors results in change in total area of circuit. There is need to design the circuit in such a way that reduction in leakage current, power consumption and area can be minimized to maximum possible way.

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9. AUTHOR PROFILE

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