Simulation of a Nanoscale SOI TG n-FinFET

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ABSTRACT

The objective of this work is to study the electrical characteristics of a nanoscale SOI Tri-Gate n-channel fin field-effect transistor (FinFET) structure with 8 nm gate length using Semiconductor TCAD tools. ATLAS™ tools are computer programs which allow for the creation, fabrication, and simulation of semiconductor devices in three dimensions with different models under consideration. The drain current, transconductance, threshold voltage, subthreshold slope, leakage current, drain induced barrier lowering, and I_{On}/I_{Off} current ratio are analyzed in the various biasing configuration. In addition, FinFET device with a high value of gate dielectric constant exhibits much better performance compared to the Si_3N_4 dielectric material, which is desirable for high performance low-power/low-voltage applications. It is found that increasing the high-k value was beneficial in reducing the subthreshold slope, DIBL, and leakage current.

General Terms

Integrated Circuit, VLSI, FinFET Device Modeling.

Keywords

Device scaling, FinFET, SCEs, Leakage current, Silvaco Software.

1. INTRODUCTION

Miniaturization technologies of electronic components like fin-shaped field effect transistors (FinFETs) have driven much over times. The study of the advanced FinFET technology is a current topic of research for all the production companies, like TSMC, Intel, and Samsung, which are in the race to get a high performance of microprocessors beyond the barrier of 14 nm. Among all, FinFET is one of the most attractive devices for implementing nanoscale CMOS technology node applications, since this type of transistor provides a better scalability option due to its excellent immunity to short channel effects (SCEs) [1- 6]. For the FinFET, the body thickness (T_{Fin}) should be approximately half of the gate length (L_G) to provide better control of short channel effects (SCEs). The drain induced barrier lowering (DIBL), subthreshold slope (SS), and leakage current (I_{off}) increase sensibly when L_G/T_{Fin} ratio is smaller than 1.5 [2, 7]. The use of silicon on insulator substrate for manufacturing microprocessors was introduced from the major semiconductor companies with the aim to minimize parasitic capacitances and to improve current drive, circuit speed, and power consumption [1].

Increasing power consumption and degrading device performance is observed when the SiO_2 used as gate insulator [8]. Therefore, the high-k dielectric materials (Al_2O_3, La_2O_3, and ZrO_2) are considered as promising solution to improve the gate control on the channel region and electrical performance [9]. The region between the source and the drain of the considered device is covered by implementing the zirconium dioxide (ZrO_2, $\kappa = 25$) as high-κ gate dielectric materials which allow further miniaturization of electronic components [9].

This paper presents an investigation of electrical characteristics of an SOI TG n-FinFET structure with 8 nm gate length. In the simulation, the Lombardi constant voltage and temperature (CVT), Shockley Read Hall (SRH), and Auger (AUGER) models were taken into consideration. The main results of simulations have been extracted, investigated, and compared to the results of recent papers. In this way it is guaranteed that the simulated results of considered device are improved. This study has been performed for three different gate dielectrics which are Si_3N_4, Al_2O_3, and ZrO_2. It is observed that the best results are obtained when ZrO_2 is used as a gate oxide material by keeping in mind both speed and low power consumption as major targets.

2. DEVICE STRUCTURE

The 3D schematic view of the simulated triple-gate (TG) FinFET structure is shown in Fig. 1. The device dimensions, L_G, H_{FIN}, T_{FIN}, and t_{ox} are the gate length, the height of silicon fin, the thickness of silicon fin, and thickness of gate oxide, respectively. The thin ZrO_2 layer has been proposed to replace conventional SiO_2 for good gate control of SCEs.
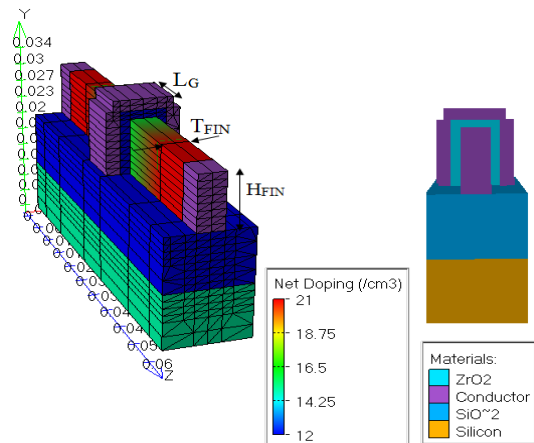

Fig. 1: The device structure of an SOI TG n-FinFET.

In TG FinFET, as depicted in Fig. 1, the gate oxide thickness is equal in all three sides of the fin region and it has been fixed at $t_{ox} = 1.5$ nm. The height of silicon fin ($H_{FIN} = 8$ nm) is defined as the distance between the top gate and bottom gate oxides. The thickness of silicon fin ($T_{FIN} = 4$ nm) is defined as the distance between front gate and back gate oxides. The channel region is formed by a slightly doped volume with doping concentration 10^{16} cm^{-3} (P-type). The doping concentrations of source/drain regions are assumed to be uniform and equal to 10^{21} cm^{-3} (n-type). The value of the gate work function is 4.53 eV.

3. DEVICE SIMULATION USING SILVACO-ATLAS

The numerical device simulator, ATLAS™ has been used to simulate the structure of the proposed SOI TG n-FinFET with high-k material. A numerical simulation in SILVACO consists of two main steps: the structure creation and numerical resolution. The structure creation includes the definition of the mesh, the different regions of the device, electrodes, and doping, while the numerical resolution includes the definition of the gate work function, the choice of physical models, and mathematical methods used by the simulator [10]. The choice of physical models is important to improve the accuracy of the numerical simulation results. In this simulation, the inversion-layer Lombardi constant voltage and temperature mobility model was considered. Auger model is invoked to deal with the minority carrier recombination. The Shockley Read Hall generation and recombination model have also been used. Two numerical methods Gummel and Newton are invoked to attain the results [10]. The simulations were carried out setting the device temperature at T = 300 K.
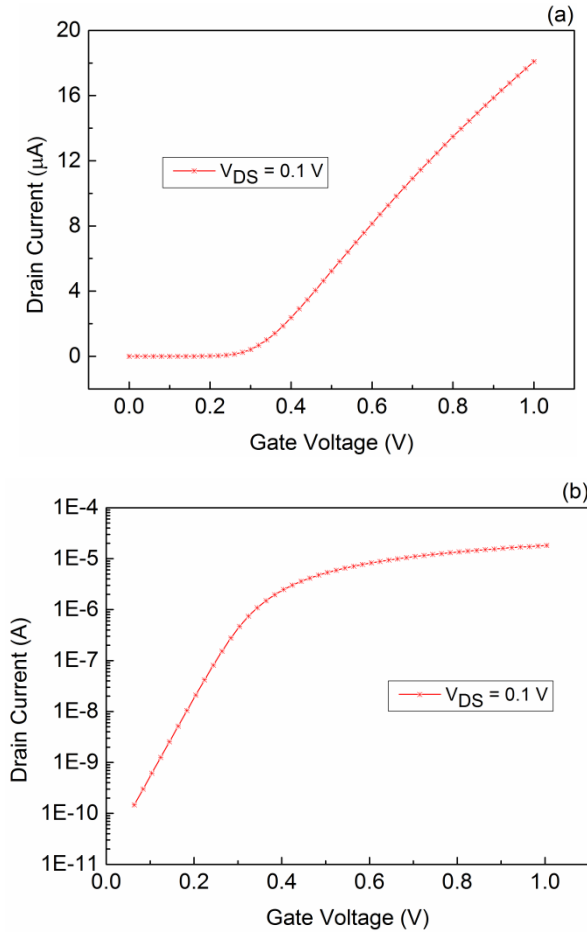
Fig. 2: Linear (a) and log scale (b) of simulation drain current (I_{DS}) versus gate voltage (V_{GS}) for TG FinFET device.

In Fig. 2, I_{DS}-V_{GS} characteristics are shown on a linear scale (a) and log scale (b) for a TG n-FinFET device structure. The gate voltage V_{GS} is swept from 0 to 1 V in steps of 0.02 V. In Fig. 2 (a), it is observed that the threshold voltage (V_{th}) of the device is 0.27 V at $V_{DS} = 0.1$ V. This parameter is good compared to the one obtained by Baravelli et al. (i.e., 0.36 V) [11]. There were some modifications at the level of the work functions of the metal gates to reach the V_{th} value desired. The

threshold voltage expression in case of a MuGFET (MultiGate Field-Effect Transistor) device structure can be expressed as [1]:

$$V_{Th} = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} + \frac{Q_{SS}}{C_{ox}} + V_{in} \qquad (1)$$

where Q_{ss} represents the charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, Φ_{ms} represents the metal-semiconductor work function difference between the gate electrode and the semiconductor, and Φ_f is the Fermi potential which for P-type silicon is given by:

$$\Phi_f = \frac{KT}{q} \ln \frac{N_A}{n_i} \qquad (2)$$

where K is the Boltzmann constant, T is the temperature, q is the electron charge, N_A is the acceptor concentration in the p-substrate, and n_i is the intrinsic carrier concentration.

When a dielectric material is inserted, the capacitance increases by the relative dielectric constant κ. In this case, the capacitance is described by eq. (3) [11]:

$$C_{ox} = \frac{\kappa \varepsilon_0 A}{t_{ox}} \qquad (3)$$

where κ is the dielectric constant of the material (κ = ε/ε$_0$), ε$_0$ is the permittivity of free space, and t_{ox} is the thickness of dielectric layer.

The critical electrical parameters such as subthreshold slope and drain-induced barrier lowering are defined as:

$$SS \ (mV/dec) = \frac{d\,V_{GS}}{d(\log_{10} I_{DS})} \qquad (4)$$

$$DIBL \ (mV/V) = \frac{\Delta V_{Th}}{\Delta V_{DS}} \qquad (5)$$

The subthreshold slope is defined as the change in gate voltage that must be applied in order to create a one decade increase in the output current [2]. The lowest theoretical limit for SS is 60 mV/decade at room temperature [12, 13]. The subthreshold slope of the considered device is 63.93 mV/decade at $V_{DS} = 0.1$ V, as depicted in Fig. 2 (b).

The DIBL is defined as the ratio of the difference in threshold voltage measured at a low value to high value of the drain voltage [2]. In this case, DIBL is 34.87 mV/V for V_{th} at $V_{DS} = 0.01$ V (V_{DS} Low) and $V_{DS} = 0.05$ V (V_{DS} High) of the SOI TG n-FinFET device.

The Subthreshold slope and drain induced barrier lowering of the considered SOI TG n-FinFET device with $L_G = 8$ nm, $T_{FIN} = 4$ nm, and $H_{FIN} = 10$ nm (i.e., 63.93 mV/dec and 34.87 mV/V) show improvement compared to TG FinFET device with $L_G = 20$ nm, $T_{FIN} = 8$ nm, and $H_{FIN} = 25$ nm (i.e., 71.82 mV/dec and 35.53 mV/V) and $L_G = 16$ nm, $T_{FIN} = 8$ nm, and $H_{FIN} = 32$ nm (i.e., 70 mV/dec and 70 mV/V) [2, 14], respectively. All the minimum values of these device parameters are required for small size of the transistor. Furthermore, transistor dimensions scale to minimize parasitic capacitances, to reduce power consumption, and to improve

current drive, and circuit speed.

The simulated transconductance exhibits roughly the same shape with different maximum value at different drain-source voltages. In particular, the transconductance first increases and then decreases by increasing the gate voltage, as shown in Fig. 3. The transconductance can be expressed as [15]:

$$g_m = \frac{d\, I_D}{dV_{GS}} \qquad (6)$$

The transconductance g_m quantifies the drain current variation due to a gate-source voltage variation while keeping the drain-source voltage constant [15]. Therefore, the value of g_m is extracted by taking the derivative of the I_{DS}-V_{GS} curve. The obtained maximum value is 29.54 µA/V of a TG n-FinFET device with 8 nm gate length at $V_{DS} = 0.1$ V and $V_{GS} = 0.5$ V, as it is shown in Fig. 3.
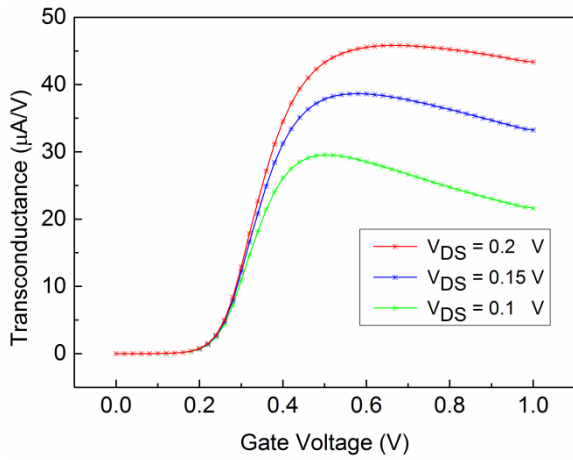

Fig. 3: Transconductance versus V_{GS} for a TG n-FinFET device at different drain-source voltages.
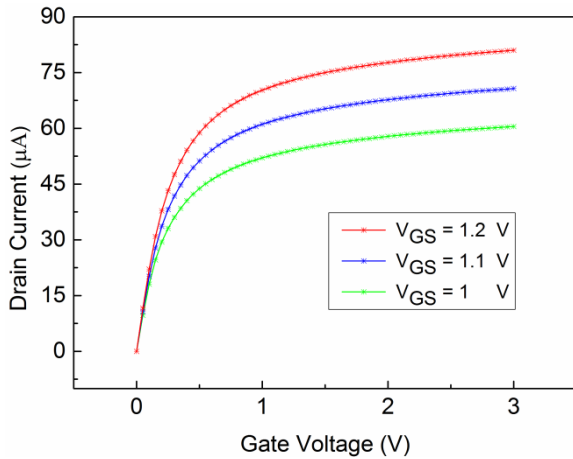

Fig. 4: I_{DS}-V_{DS} characteristics for an SOI n-FinFET at different gate voltages.

Fig. 4 illustrates output characteristics depending on gate-source voltage of n-channel FinFET. The curves present the relationship between drain current and drain to source voltage for different values of gate-source voltage. First, it is found that the increasing V_{GS} will result in a higher channel conductivity, which means a lower channel resistivity. Fig. 5 shows the variation of the drain current with the gate to source voltage for different drain to source voltages.
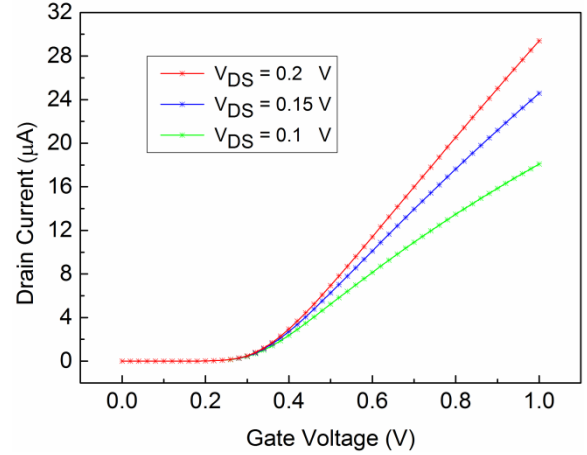

Fig. 5: I_{DS}-V_{GS} characteristics on a linear scale for an SOI n-FinFET device at different drain-source voltages.

The threshold voltage is a very important parameter for obtaining a higher on-current, which improves the circuit speed. At room temperature, it is found that the on-current output is 52 µA at $V_{GS} = V_{DS} = V_{DD}$ and $V_{DS} = 1$ V as shown in the Fig. 6, where V_{DD} is the supply voltage. Furthermore, I_{DS} is calculated as reported by the following formula [16]:

$$I_{DS}\,(nA) = 100\ \frac{W}{L}\ e^{\frac{q(V_{GS}-V_{Th})}{\eta KT}} \qquad (7)$$

where W is the width of the channel, L is the channel length, Q is the electronic charge, and η is the body factor, which is proportional to the change in gate voltage with a change in channel potential [16].
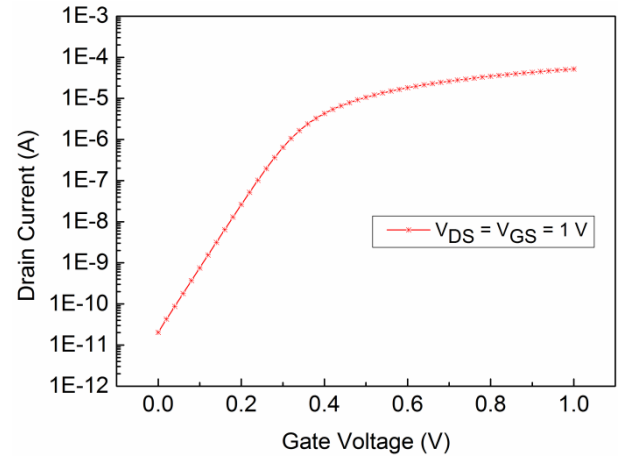

Fig. 6: I_{DS}-V_{GS} characteristics on a log scale for an SOI n-FinFET at $V_{DS} = 1$ V.

The leakage current is directly related to the SS. Fig. 6 shows, that the leakage current output is 20.41 pA at $V_{GS} = 0$ V and $V_{DD} = V_{DS} = 1$ V. I_{off} has been calculated by the following formula [16]:

$$I_{off}\,(nA) = 100\ \frac{W}{L}\ 10^{\frac{-V_{Th}}{SS}} \qquad (8)$$

The leakage current and subthreshold slope of the considered device (i.e., 20.41 pA and 63.93 mV/decade) are excellent

compared with the results of the recent paper [17], reporting on a gate-all-around MOSFET with L_G = 20 nm, T_{FIN} = 12 nm, H_{FIN} = 24 nm (i.e., 700 pA and 86.73 mV/dec), even with a smaller physical L_G. It is important to keep I_{off} very small, in order to minimize the static power dissipation even when the device is in the standby mode. The ratio I_{on}/I_{off} exceeds 10^6 for the analysed device with ZrO_2 as gate dielectric material at room temperature [15], which indicates the excellent on-state and off-state characteristics compared with the results of the recent paper reporting on a 20 nm conventional FinFET (i.e., $7.42 \; 10^3$) [18].

4. EFFECT OF GATE DIELECTRIC MATERIALS

The gate dielectric materials play a key role in the design of novel and high performances at nanoscale of electrical devices. It is well-known that high-κ materials are more suitable than the well-known SiO_2 due to the smaller thickness required which decreases the threshold voltage and improves the leakage characteristics of the device. This simulation has been performed for three different gate dielectrics which are silicon nitride (Si_3N_4, κ = 7.55), aluminium oxide (Al_2O_3, κ = 9), and zirconium dioxide (ZrO_2, κ = 25) [9]. The dependencies of subthreshold slope and DIBL on the gate dielectric constant (κ) for TG n-FinFETs are shown in Figs. 7 and 8, respectively.
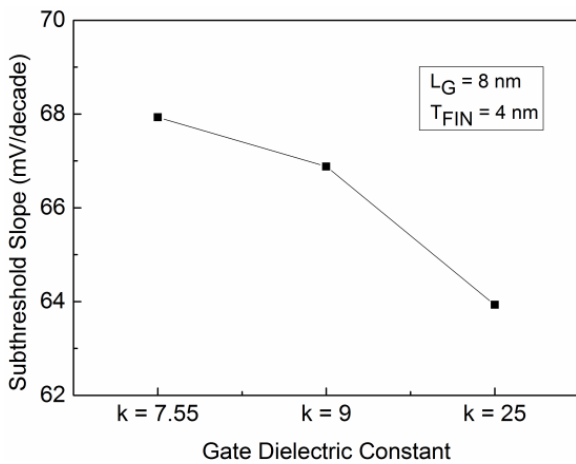
Fig. 7: Subthreshold slope variation for different gate dielectrics at V_{DS} = 0.1 V.
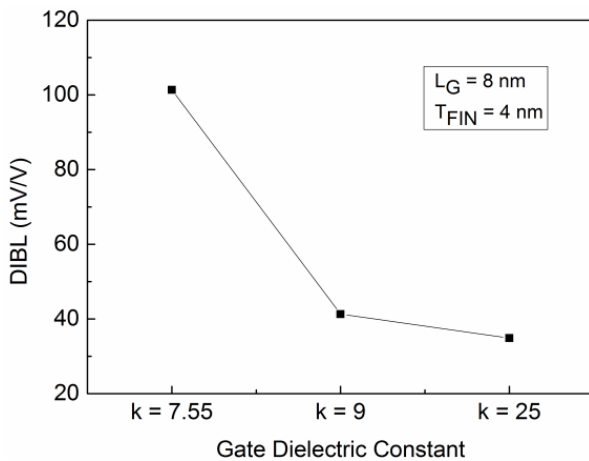
Fig. 8: DIBL variation for different gate dielectrics.

Initially, subthreshold slope decreases with the increase of high-k gate dielectrics. Afterwards, swing starts decreasing and comes close to its theoretical limit, which is shown in Fig. 7. This observation indicates that, higher value of gate dielectrics constant is desired in order to have fast n-FinFET response. Furthermore, DIBL decreases as gate dielectric constant increases. During accurate circuit design, the first important step is to get rid of these DIBL effects of the transistor. FinFET device with physical gate length of 8 nm has been optimized for low leakage current when the value of gate dielectrics increases by keeping the fin thickness minimum ($\approx L_G/2$), as depicted in Fig. 9.
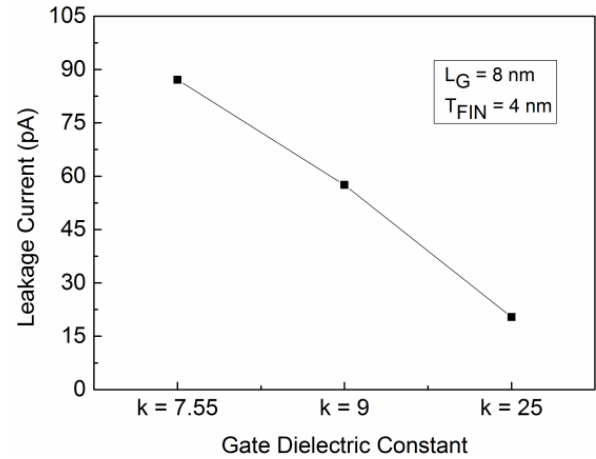
Fig. 9: Leakage current variation for different gate dielectrics at V_{GS} = 0 V and V_{DS} = 1 V.

Figs. 10 and 11 illustrate the On-current and I_{On}/I_{Off} ratio characteristics with different gate dielectric constants for an SOI TG n-FinFET, respectively. I_{On} is also significant for device performance. Furthermore, the variation of transconductance with different gate dielectrics at the gate-source voltage V_{GS} for which $g_{m \; max}$ is simulated. It can be seen that transconductance increases with the increase of dielectric constant as shown in Fig. 12. All these characteristics improve with an increase of dielectric constant κ, it can be observed that the best results are obtained when ZrO_2 is used as a gate dielectric.
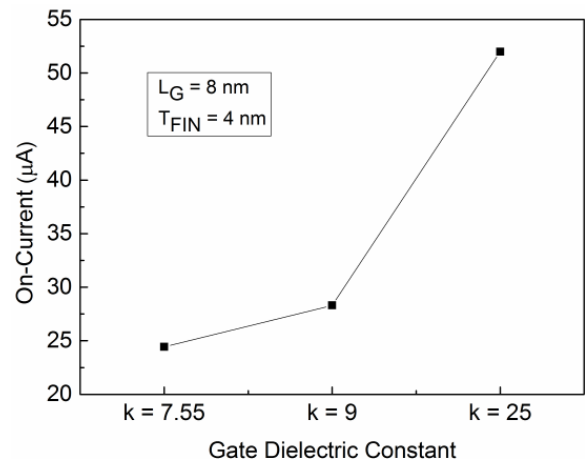
Fig. 10: On-current variation for different gate dielectrics at V_{GS} = V_{DS} = 1 V and V_{DS} = 1 V.
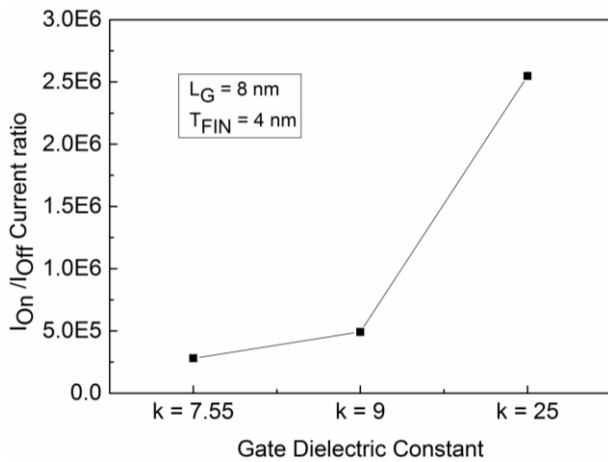
Fig. 11: I_{On}/I_{Off} current ratio for different gate dielectrics.
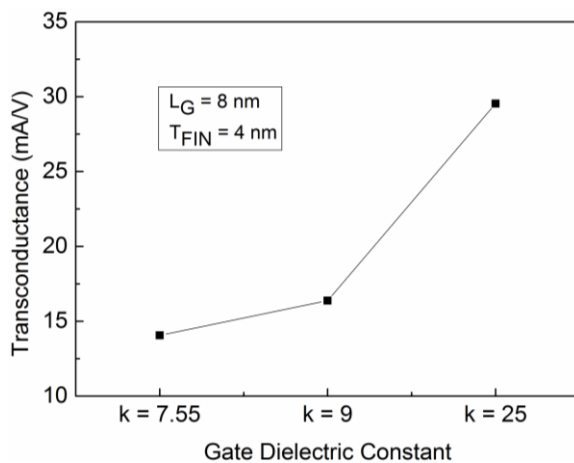

Fig. 12: Maximum transconductance variation for different gate dielectrics at V_{DS} = 0.1 V.

5. CONCLUSION

Tri-Gate n-channel fin field-effect transistor structure has been simulated. This device exhibited good performance characteristics down to 8 nm by using ZrO_2 as gate dielectric material. The device geometry requires inclusion of specific models to extract different electrical characteristics such as drain current, transconductance, threshold voltage, subthreshold slope, leakage current, drain induced barrier lowering, and I_{On}/I_{Off} current ratio. An increased value of κ improves electrical device characteristics. By achieving better values of DIBL and SS of the device, n-channel FinFETs showed good short-channel performance down to 8 nm gate length, allowing more efficient reduction of the leakage characteristics. It can be concluded that this study produces different results which may be useful to the further manufacturing process.

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