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Effects of High-k Dielectric Materials on Electrical Characteristics of DG n-FinFETs

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ABSTRACT
This paper investigates the electrical characteristics of the nanoscale n-channel double gate fin field-effect transistor (FinFET) structures and their sensitivity to gate dielectric materials with different channel materials using SiGe and 3C-SiC in the channel region. In this work, the numerical tool Atlas Silvaco was used to simulate the device in three dimensions and evaluate the electrical characteristics of the device at 300K. The influence of the gate dielectrics on threshold voltage roll-off, subthreshold slope, transconductance, drain induced barrier lowering, leakage current, on-current, and on/off current ratio has been investigated. The simulation results show that high drain current and transconductance were obtained with SiGe channel material. The results also show that a higher value of gate dielectric constant can increase the drain current and improve the leakage current. Drain induced barrier lowering is reduced with the increase in gate dielectric constant. It can be noticed with different and useful results which led researchers to further manufacturing process in order to get the complete device.

General Terms
Integrated Circuit, VLSI, FinFET Device Modeling.

Keywords
Nanoscale, Double gate, FinFEts, SCEs, DIBL, Silvaco Software.

1. INTRODUCTION
The new technology is oriented towards the miniaturization of electronic components and transistors in integrated circuits. The goal is to integrate more components per unit area and thus improve circuit performance while lowering their manufacturing cost as predicted by the “Moore’s Law” [1].

The multi-gate transistors like FinFETs (Fin-Shaped Field Effect Transistor) are considered to be the best candidates to extend the use of CMOS technology beyond the barrier of 14 nm. Double-gate FinFET is considered one of the most promising device structures for future CMOS technology, which provides a better electrical control over the channel and thus allows increasing the device performances [2- 5].

For the FinFET, the body thickness T_{Fin} should be approximately half of the gate length L_G to provide better control of short channel effects (SCEs). The drain induced barrier lowering, subthreshold slope, and leakage current increase sensibly when L_G/T_{Fin} ratio is smaller than 1.5 [2, 4].

SiGe is an attractive material for advanced CMOS technology due to its enhanced carrier mobility in which the threshold voltage of the SiGe-channel device appears to be smaller with higher drain conductance and higher transconductance compared with Si-channel device [6].

Silicon carbide (SiC) also is a very promising semiconductor due to its physical and electrical properties, it has excellent material properties which make it superior to Si in a wide range of applications. SiC is an ideal choice for manufacturing devices designed to work at high temperature, high power, and high voltage. These properties have garnered increased interest in the use of SiC in many high-performances in micro/nano-technology devices and they are better for 3C-SiC (heteroepitaxial) than for the hexagonal SiC (4H- and 6H-) [7].

The new research introduces the use of high-κ gate materials to manufacture an electrical device in order to improve the current drive and to minimize the gate leakage current which decreases the power consumption. The reason behind using high-κ dielectrics is to improve the electrical characteristics of the device [8].

This paper presents a numerical investigation of nanoscale double gate n-FinFET with the channel made either of SiGe or 3C-SiC. In the simulation, the Shockley–Read–Hall (SRH) and Auger (AUGER) models were considered [9]. The influence of the gate dielectric materials on threshold voltage (V_{th}), subthreshold slope (SS), transconductance (g_m), drain induced barrier lowering (DIBL), leakage current (I_{off}), on-current (I_{on}), and On/Off current ratio has been investigated. This study has been performed for four different gate dielectrics which are SiO_2, Si_3N_4, Al_2O_3, and ZrO_2. It can be observed that the best results are obtained when ZrO_2 is used as a gate oxide material by keeping in mind either speed and power consumption as major targets.

2. DEVICE STRUCTURE
The schematic structure used for these simulations is represented in Fig. 1. The different parameters of the structure are assumed as follows in table 1.

Table 1: Parameters of symmetrical DG n-FinFET.

Symbol	Designation	Value
L_D, L_S	Drain length and Source length (Silicon material)	11 [nm]
L_G	Gate length	8 [nm]
L_{ch}	Channel length (SiGe / 3C-SiC material)	10 [nm]
T_{OX} (ZrO_2)	Lateral oxide thickness (gate dielectric material)	1.5 [nm]
T_{FIN}	Fin thickness	4 [nm]

H_{FIN}	Fin Height	10 [nm]
N_A	Channel concentration	10^{16} [cm^{-3}]
N_D	Drain and Source concentration	10^{21} [cm^{-3}]

The DG-FinFET technology is based on vertical silicon fin characterized by the fin length (L_G), fin height (H_{FIN}), and the fin-thickness (T_{FIN}) as shown in Fig. 1 [10]. The channel region is formed by a little doped with doping concentration 10^{16} cm^{-3} (P-type). The doping concentrations of source/drain regions are assumed to be uniform and equal to 10^{21} cm^{-3} (n-type). The value of the gate work function is 4.6 eV. Fig. 1 describes the structure of a DG n-FinFET.

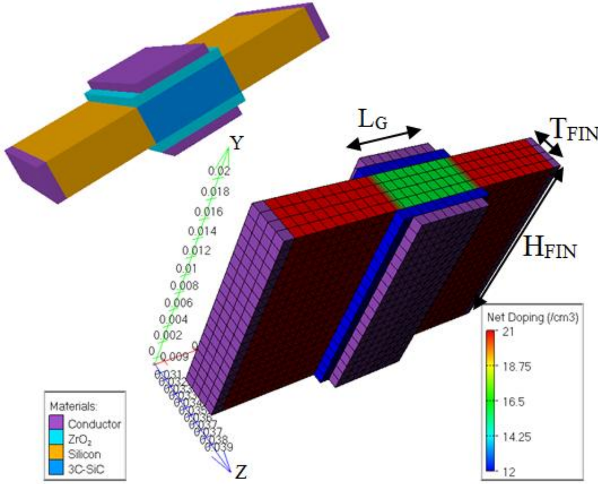

Fig. 1: Illustrates the device structure of a DG n-FinFET in 3-D.

3. DEVICE SIMULATION USING ATLAS

The software package Silvaco-Atlas was used to design, examine, and simulate the structure and characteristics of the DG-FinFET device in three dimensions. The standard recombination models like Shockley–Read–Hall and Auger models were considered in the ATLAS simulation [9]. In Figs 2 and 3, I_{DS}-V_{GS} transfer characteristics are shown on a linear scale and log scale for a double gate n-FinFET device structure. In Fig. 2, it is observed that the threshold voltage of a DG n-FinFET is 0.4 V with 3C-SiC channel material and 0.38 V with SiGe channel material at V_{DS} = 0.1 V. The threshold voltages obtained are excellent values compared to the one obtained by Guangxi et al. [11]. The simulation shows that the drain current of SiGe channel is larger than the current of 3C-SiC channel by about 0.54 mA respect to a n-FinFET device at V_{GS} = 1 V. The threshold voltage expression in case of a multigate field-effect transistor (MuGFET) device structure can be expressed as [1]:

$$V_{Th} = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} + \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (1)$$

Where Q_{ss} represents charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, Φ_{ms} represents metal-semiconductor work function difference between the gate electrode and the semiconductor and Φ_f is the Fermi potential which for P-type silicon given by:

$$\Phi_f = \frac{KT}{q} ln \frac{N_A}{n_i} \quad (2)$$

Where k is the Boltzmann constant, T is the temperature, q is the electron charge, N_A is the acceptor concentration in the p-substrate, and n_i is the intrinsic carrier concentration.

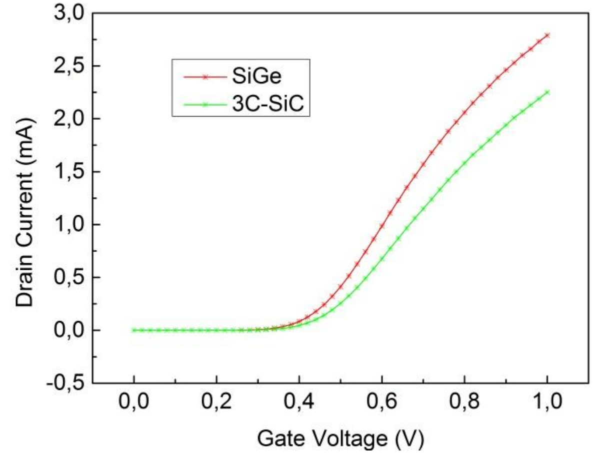

Fig. 2: I_{DS}-V_{GS} characteristics on a linear scale for a DG n-FinFET at V_{DS} = 0.1 V.

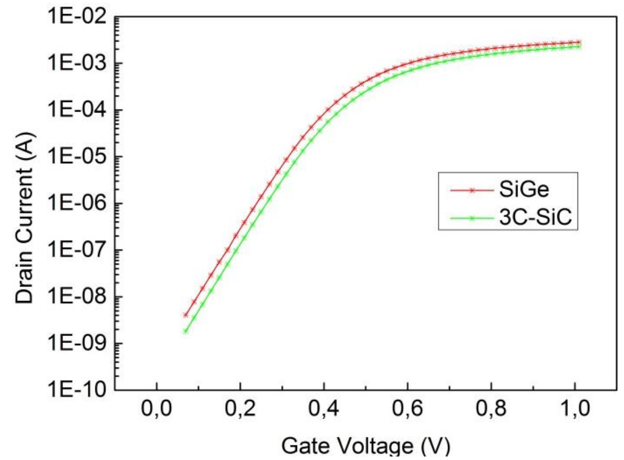

Fig. 3: I_{DS}-V_{GS} characteristics on a log scale for a DG n-FinFET at V_{DS} = 0.1 V.

When a dielectric material is inserted between the metal gate and semiconductor material, the capacitance increases by the relative dielectric constant κ. In this case, the capacitance is described by [8]:

$$C_{ox} = \frac{\kappa \varepsilon_0 A}{t_{ox}} \quad (3)$$

Where κ is the dielectric constant of the material ($\kappa = \varepsilon/\varepsilon_0$), ε_0 is the permittivity of free space, t_{ox} is the thickness of dielectric layer.

The transconductance g_m quantifies the drain current variation with a gate-source voltage variation while keeping the drain-source voltage constant [4, 12]

$$g_m = \frac{d\, I_D}{dV_{GS}} \quad (4)$$

Therefore, the value of g_m is extracted by taking the derivative of the I_{DS}-V_{GS} curve, the obtained value is 4.82 mA/V of a

DG n-FinFET with 3C-SiC channel material and 6.12 mA/V of a DG n-FinFET with SiGe channel material at $V_{DS} = 0.1$ V and $V_{GS} = 0.6$ V.

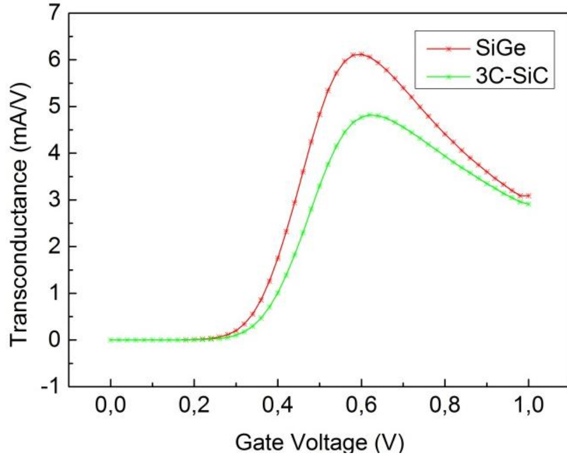

Fig. 4: Transconductance versus V_{GS} for a DG n-FinFET at $V_{DS} = 0.1$ V.

Fig. 4 shows the transconductance characteristics of a DG n-FinFET with two different channel materials at $V_{DS} = 0.1$ V. As can be seen in the Fig. 4, also the maximum transconductance of SiGe channel is higher than that of 3C-SiC channel by approximately 1.3 mA/V. These results reflect the faster carrier transport due to SiGe channel material with shorter gate length device (8 nm gate length). On the other hand, the transconductance decreases rapidly with increasing positive V_{GS} for both SiGe and 3C-SiC channel materials. The transconductance of the both considered DG n-FinFET devices with $L_G = 8$ nm, $T_{FIN} = 4$ nm, and $H_{FIN} = 10$ nm show an improvement compared to Trigate Wavy FinFET device with $L_G = 20$ nm, $T_{FIN} = 7$ nm, and $H_{FIN} = 25$ nm [13]

The subthreshold slope is the major parameter for calculating the leakage current. Furthermore, SS is calculated as in [4, 12]:

$$SS\,(mV/dec) = \frac{d\,V_{GS}}{d(\log_{10} I_{DS})} \tag{5}$$

A typical value for the SS parameter of a MuGFET is 60 mV /decade, (i.e., a 60 mV change in gate voltage brings about a tenfold change in drain current) [9, 12]. The subthreshold slope of the considered device is 69.50 mV/decade with SiGe channel material and 69.05 mV/decade with 3C-SiC channel material at $V_{DS} = 0.1$ V, as it is shown in Fig. 3. The Subthreshold slope of the considered DG n-FinFET device with $L_G = 8$ nm, $T_{FIN} = 4$ nm, and $H_{FIN} = 10$ nm show improvement compared to TG FinFET device with $L_G = 20$ nm, $T_{FIN} = 8$ nm, and $H_{FIN} = 25$ nm (i.e., 71.82 mV/dec) and $L_G = 16$ nm, $T_{FIN} = 8$ nm, and $H_{FIN} = 32$ nm (i.e., 70 mV/dec) [2, 14], respectively. All the minimum values of these device parameters are required for small size of the transistor. Furthermore, transistor dimensions scale to minimize parasitic capacitances, to reduce power consumption, and to improve current drive, and circuit speed.

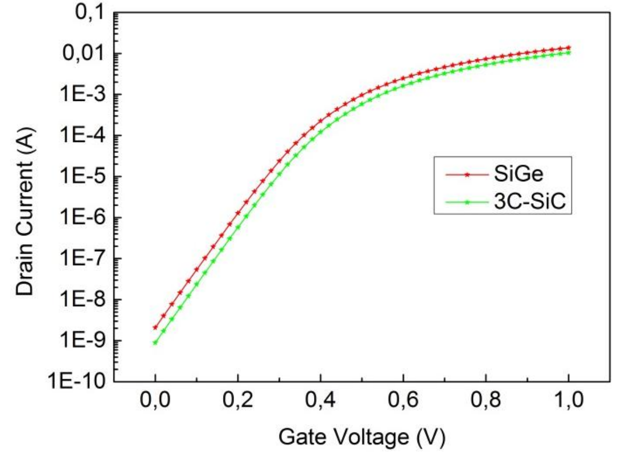

Fig. 5: I_{DS}-V_{GS} characteristics on a log scale for a DG n-FinFET at $V_{GS} = V_{DS} = V_{DD}$ and $V_{DS} = 1$ V.

The threshold voltage is a very important parameter for obtaining a higher on-current, which improves the circuit speed. In Fig. 5, it is observed that the on-current output is 10.35 mA with 3C-SiC channel material and 13.64 mA with SiGe channel material at $V_{GS} = V_{DS} = V_{DD}$ and $V_{DS} = 1$ V. Furthermore, I_{DS} is calculated as reported in [4, 12]:

$$I_{DS}\,(nA) = 100\,\frac{W}{L}\,e^{\frac{q(V_{GS}-V_{Th})}{\eta KT}} \tag{6}$$

In Fig. 6 the measured output characteristics of DG n-FinFET is shown. The highest drain current is obtained by using SiGe material as the channel material.

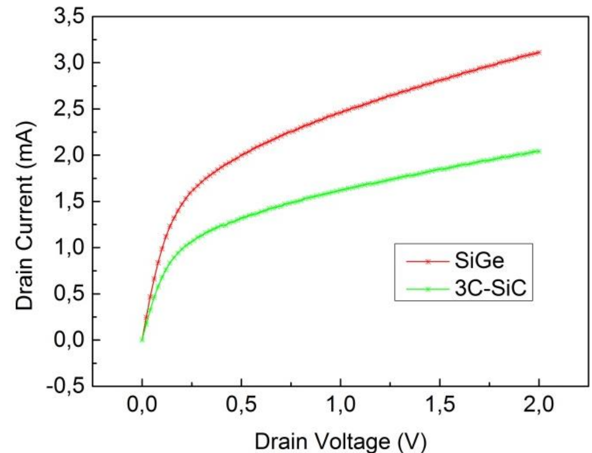

Fig. 6: I_{DS}-V_{DS} characteristics for a DG n-FinFET at different channel material.

The leakage current is directly related to the SS. Fig. 5 shows that the drain leakage current is 0.89 nA with 3C-SiC channel material and 2.08 nA with SiGe channel material at $V_{GS} = 0$ V and $V_{DD} = V_{DS} = 1$ V. I_{off} calculated by the formula in [4, 12]:

$$I_{off}\,(nA) = 100\,\frac{W}{L}\,10^{\frac{-V_{Th}}{SS}} \tag{7}$$

The leakage current of the both considered DG n-FinFET devices show an improvement compared with the results of the recent paper [15], reporting on a Trigate Wavy FinFET device [15].

It is important to keep I_{off} very small, in order to minimize the static power dissipation even when the device is in the standby mode. The ratio I_{on}/I_{off} exceeds 10^6 for the analyzed devices at room temperature, which indicates the excellent on-state and off-state characteristics compared with the results of the recent paper reporting on a 20 nm conventional FinFET (i.e., 7.42 10^3) [13].

The value of the drain induced barrier lowering (DIBL) is calculated by using the relation reported in [4, 12]:

$$DIBL\ (mV/V) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \qquad (8)$$

The DIBL is defined as the difference in threshold voltage when the drain voltage is increased from 0.05 V to 0.1 V. In this case, DIBL is 71.1 mV/V with 3C-SiC channel material and 81.46 mV/V with SiGe channel material for the DG n-FinFET at 8 nm gate length.

4. EFFECT OF GATE DIELECTRIC MATERIALS

The gate dielectric materials have played significant role in the design of novel and high performances at nanoscale of electrical devices. It is well-known that high-κ materials are more suitable than the well-known SiO_2 due to the smaller thickness required which decreases the threshold voltage and improves the leakage characteristics of the device. Fig. 7 illustrates the subthreshold slope variation for four different gate dielectrics which are silicon oxide (SiO_2, κ = 3.9), silicon nitride (Si_3N_4, κ = 7.55), aluminum oxide (Al_2O_3, κ = 9), and zirconium dioxide (ZrO_2, κ = 25) [8]. Both subthreshold slope and DIBL decrease as gate dielectric constant decreases for two channel materials (SiGe, 3C-SiC) as shown in the Figs 7 and 8, respectively.

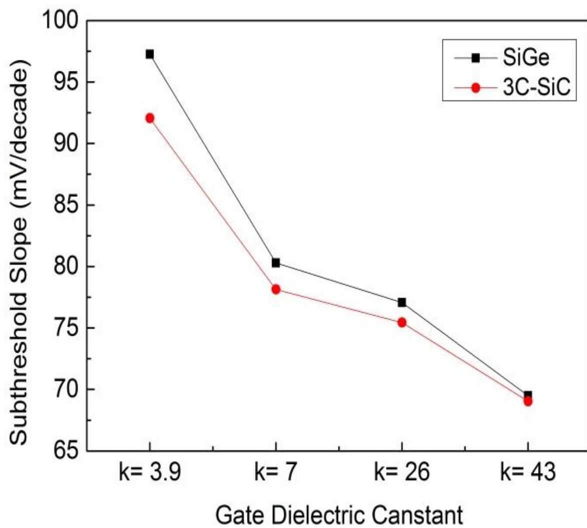

Fig. 7: Subthreshold slope variation for different gate dielectrics at V_{DS} = 0.1 V.

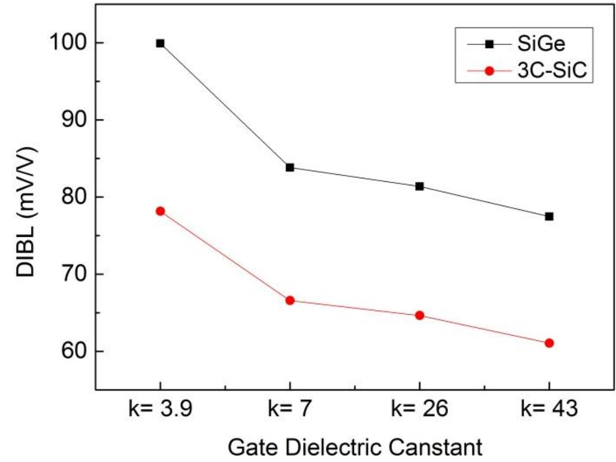

Fig. 8: DIBL variation for different gate dielectrics at V_{DS} = 0.1 V.

Fig. 9 shows the variation of transconductance with different gate dielectrics at the gate-source voltage V_{GS} for which $g_{m\ max}$ is simulated. It can be seen that transconductance increases with the increase of dielectric constant. It can be concluded, as already started, that the channel mobility is higher with a SiGe material, which reduces the parasitic and access resistance.

Figs 10-12 illustrate the On-current, Off-current, and I_{On}/I_{Off} ratio characteristics with different gate dielectric constants for a DG n-FinFET, respectively. All these characteristics improve with an increase of dielectric constant κ; it can be observed that the best results are obtained when ZrO_2 is used as a gate dielectric. I_{On} is also significant for device performance, I_{On} of SiGe channel material is higher as much as this of 3C-SiC channel material. Therefore, it can be concluded that the SiGe channel material can be used to achieve higher on-current than that of 3C-SiC channel material.

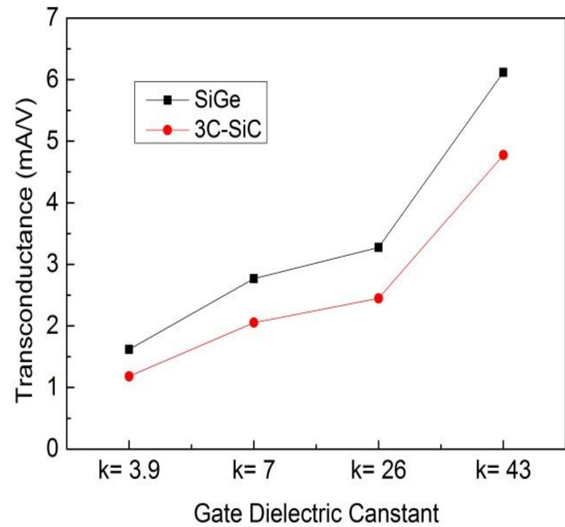

Fig. 9: Transconductance variation for different gate dielectrics at V_{DS} = 0.1 V.

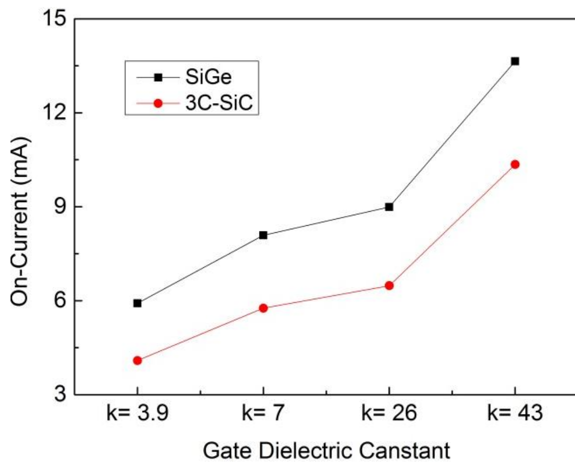

Fig. 10: On-current variation for different gate dielectrics at $V_{GS} = V_{DS} = V_{DD}$ and V_{DS} = 1 V.

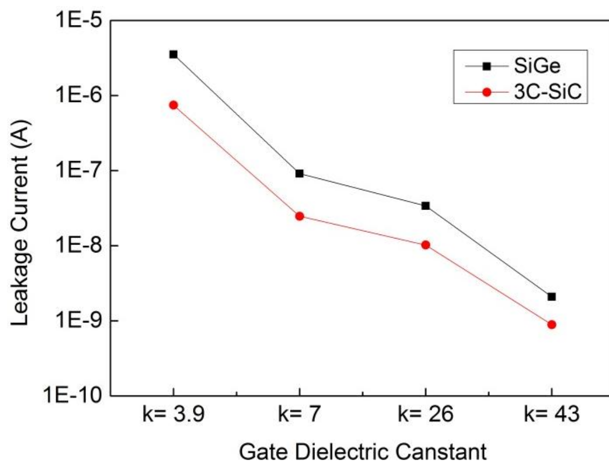

Fig. 11: Leakage current variation for different gate dielectrics at V_{GS} = 0 V and $V_{DD} = V_{DS}$ = 1 V.

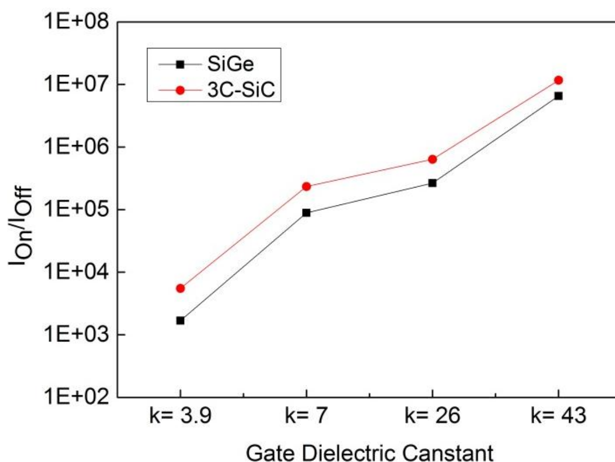

Fig. 12: On/Off current ratio for different gate dielectrics.

5. CONCLUSIONS

In this work, the numerical simulation tool Atlas Silvaco has been used to design, examine, and simulate the two different channel materials of DG n-FinFETs with different gate dielectric materials. As indicated by the three-dimensional simulation results, the carrier mobility of SiGe channel device is higher which the threshold voltage appears to be smaller with higher drain conductance and higher transconductance compared with 3C-SiC channel device. An increased value of κ improves electrical device characteristics.

This nanometer gate device has thus shown to provide improved control of the channel, allowing more efficient reduction of the leakage current at 8 nm gate length.

6. REFERENCES

[1] J-P. Colinge, 2008 FinFETs and Other Multi-Gate Transistors, *New York: Springer US*, p 355.

[2] Narendar, V. and Mishra, R. A. 2015 Analytical modeling and simulation of multigate FinFET devices and the impact of high-k dielectrics on short channel effects (SCEs), *Superlattices Microstruct.*, 85, 357-369.

[3] D. Hisamoto, et al, 2000 FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm, *IEEE Trans. Electron Devices,* vol. 47**,** 2320-2325.

[4] N. Boukortt, et al., 2015 3-D Simulation of Nanoscale SOI n-FinFET at a Gate Length of 8 nm Using ATLAS SILVACO, *Trans. Electr. Electron. Mater.* vol. 16, 2-7.

[5] N. Boukortt, B. Hadri, and A. Caddemi, 2016 Simulation of a Nanoscale SOI TG nFinFET, *Int J Comput Appl.,* Vol. 138, 10-14.

[6] C. R. Selvakumar, et al, 1991 SiGe-Channel n-MOSFET by Germanium Implantation, *IEEE Electron Device Lett,*. vol. 12**,** 444-446.

[7] G. S. Chung, et al, 2010 Electrical characterization of Au/3C-SiC/n-Si/Al Schottky junction *J. Alloys Compd.* vol. 507**,** 508-512.

[8] R. P. Ortiz, et al, 2010 High-*k* Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors, *Chem. Rev.* vol. 110**,** 205-239.

[9] S. International, 2012 Atlas User's Manual Device Simulation Software (*Silvaco Int., Santa Clara*).

[10] C. Meinhard, et al, 2014 Predictive evaluation of electrical characteristics of sub-22 nm FinFET technologies under device geometry variations, *Microelectron. Reliab.* vol. 54**,** 2319-2324.

[11] G. Hu, et al. 2016 Analytical models for channel potential, threshold voltage, and subthreshold swing of junctionless triple-gate FinFETs, *Microelectr J*. vol. 50, 60–65.

[12] S. K. Mohapatra, et al, 2013 Some Device Design Considerations to Enhance the Performance of DG-MOSFETs, *Trans. Electr. Electron. Mater.* vol. 14**,** 291-294.

[13] K. P. Pradhan et al. 2016 Exploration of symmetric high-k spacer (SHS) hybrid FinFET for high performance application. *Superlattices Microstruct.*, 90, 191-197.

[14] W. T. Huang, and Y. Li. 2015 Electrical characteristic fluctuation of 16-nm-gate trapezoidal bulk FinFET devices with fixed top-fin width induced by random discrete dopants. *Nanoscale Res Lett.*, 10:116:1-8.

[15] K. P. Pradhan, Priyanka, and P.K. Sahu 2016 Temperature dependency of double material gate oxide (DMGO) symmetric dual-k spacer (SDS) wavy FinFET. *Superlattice Microst*., 89, 355-361.