Transistor Width Size Effect on Voltage Drop and Improve Internal Resistance in CMOS Rectifier

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ABSTRACT
The proposed work based on the simulation studies for the effect of different width size of transistor on output voltage drop and internal resistance in CMOS rectifier. This paper presents the CMOS rectifier by using two PMOS and NMOS configuration and gives information about miniaturization technology. Hence, increase the width size from 4µm to 1100µm of PMOS and NMOS transistors. The results for 1100µm are 1.20V is better than 750µm width size, and also minimize the internal resistance from 6.17Ω to 4.580Ω in CMOS rectifier. The model was designed and simulated using Microwind software and operated at a frequency of 50Hz with an AC voltage source. A circuit was fabricated with 0.35µm CMOS technology.

Keywords
AC to DC converter, CMOS rectifier, width size of transistor, MOSFET internal resistance, low frequency. Voltage source.

1. INTRODUCTION
Recently, the most important technology is the miniaturization that has been increased in portable device at a large scale. It consists of several applications like transportation control, wireless network, automobiles identification. One of the main challenge for the researchers in layout designing is to reduce large voltage drop and high internal resistance. The researchers have paid attention towards the replacement of conventional rectifier which is more suitable as compare to it.

CMOS rectifier is one of the miniaturized technologies that have been proposed to replace the conventional rectifier due to having several applications. The conventional rectifier has a drawback of large voltage drop and high internal resistance. In CMOS technology, conventional rectifier and schottky diodes are not well suited, because these are not compatible with the CMOS technology. Then researchers searched a method to replace the converter by using CMOS rectifier which has lower voltage drop and low internal resistance form to the previous design. The electronic device which flows in one direction and used to convert the AC voltage to DC voltage is known as rectifier. The process is called rectification. It consists of PN junction diodes. Due to having

large numbers of applications, CMOS rectifier are useful in many different areas such as wireless network, biomedical, radio frequency identification communication area electronic portable devices like smart phones, laptops etc.

2. PROPOSED CMOS RECTIFIER
Generally, the conventional rectifiers are constructed by using diodes. But the diodes have not required for low voltage circuits and power loss is very large. Therefore, CMOS rectifier in now used because it solved all problems and reduces the forward voltage drop. The CMOS rectifier structure are simple which consist of two PMOS and NMOS transistors, is shown in the Figure 1. In this Figure M1 and M3 are PMOS transistors and M2 and M4 are NMOS transistors. For each cycle, one PMOS and NMOS will turn ON. The CMOS rectifier is used to convert a pure sinusoidal input waveforms having at a frequency of 50Hz and load resistance of 2KΩ. This larger value of load resistance increases the efficiency of CMOS rectifier. It works at a very low input voltage at 0.25V.

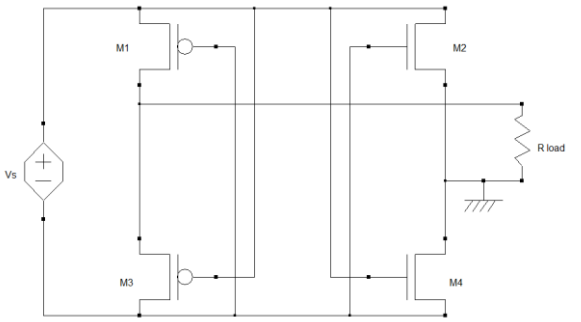

Figure.1 CMOS rectifier circuit

Although these CMOS rectifier structure are simple, By using 0.35 µm CMOS technology. This rectifier used to convert input sinusoidal wave from negative half waves into positive, which is possible with two PMOS and two NMOS transistors shown in figure 1. Hence, the voltage drop can be minimized by using large size of transistors to decrease the resistance and get a small voltage drop.

The circuit was simulated with Microwind software. The voltage efficiency is defined as the fraction of the DC output voltage V_{out} and the AC input voltage amplitude $|V_{in}|$. The efficiency of output voltage is higher with larger load resistors in CMOS rectifier. Generally the circuit cannot work when the input voltage is larger. So, in this paper we design CMOS rectifier to overcome these drawbacks. This rectifier work at a 1.5V at input voltage.

The main goals of this paper are the reduction of the voltage drop and internal resistance over the CMOS rectifier and achievement of a high efficiency. In this analysis reduce voltage drop and power loss from CMOS rectifier to the load resistor. It follows the change of the size of the MOS transistor, as the size increase, the channel resistance will become small. The voltage drop on the channel resistor will less, hence this will increase the output voltage V_{OUT}.

3. DIFFERENT PARAMETERS

For every positive cycle and negative cycle of the input AC voltage in PMOS and NMOS transistors have the internal resistance. In CMOS rectifier, when the width size of PMOS and NMOS transistors width size are increase then the total resistance is reduced. It proves that the width size is one of the factors that effect on the internal resistance and voltage drop. The transistor larger width size make the bigger current to go through to the transistor, hence it have the small value of the resistance. The width over length ratio for transistor is 750/1. The CMOS rectifier has lower internal resistance by considering the capability of electron mobility in PMOS and NMOS transistors.

3.1 Analysis of width size of transistor on internal resistance in CMOS rectifier

In this analysis, all transistor width size is set to be similar. The designs are varied from small, medium and large width sizes. Thus, the width size of PMOS and NMOS transistor is varied to improve the drive current and reduce the internal resistance in the circuit. The width size of PMOS and NMOS transistor is enlarged from 4µm to 1100µm while the length size of PMOS and NMOS transistor is set at 1µm.These analysis are done to get the lower internal resistance from 6.17Ω to 4.580Ω.

3.2 Analysis on the width size of the transistor to the output voltage in CMOS rectifier

The focused on this design is to determine the output voltage using 1100µm large width size of transistor is better than 750µm small width size of transistor. It means that the bigger width gives better output voltage 1.20V compared to lower width gives 0.61V.

3.3 Analysis of Power Conversion Efficiency dependence on transistor sizing

This analysis shows PCE dependence on the width size of transistor. The wider version exhibits a slightly larger peak PCE, where width size of PMOS and NMOS transistor is varied from lower to higher. PCE of the rectifier is defined by output power P_{OUT} divided by the input power P_{IN}. The sum of the output power and the loss of the rectifier is define the total input power. PCE can be written as:

$PCE = P_{OUT} / P_{IN}$

$PCE = P_{OUT} / (P_{OUT} + P_{LOSS})$

4. SIMULATION RESULTS AND DISCUSSION

From the CMOS rectifier design, the effect of width size was studied. Three different values of width were set in this study at 4µm, 750µm and 1100µm. The length of PMOS and NMOS transistors is set constant at 1µm to determine the effect of the width. Hence, the output waveform was analyzed. For every positive and negative cycle of the input voltage, the transistors will represent as diodes which have the internal resistance. In table 1 shows the PMOS and NMOS different width sizes. For the analysis of similar width size 4µm of transistor, design 1 have the very large internal resistance at 1570.00Ω and the maximum output voltage is only about 15mV lower compared to the input voltage. A slight delay can be observed of about 5ns. This delay can be reduced by increasing the width size of PMOS and NMOS transistor. The main aspects of rectifier are the maximum output voltages which can be reached at 1.21V, and for the study of enlarging the transistor width size, design 3 have the total resistance at 4.580Ω compared to 6.170Ω for design 2.

Table 1. Output voltage and Total Internal Resistance for similar width size in CMOS rectifier

Design	Design of CMOS rectifier (PMOS/NMOS)	Total Internal Resistance	Output Voltage
1	4µm/4µm	1570.00Ω	15mV
2	750µm/750µm	6.170Ω	0.61V
3	1100µm/1100µm	4.580Ω	1.20V

The simulation results of CMOS rectifier circuit will be shown below. The output voltage could reach 1.20V. However the structure, which helps to reduce the voltage drop, power loss and minimize internal resistance. Also reduce the chip area in MOSFET. The input voltage is set to 1.5V at the voltage source and the sine waveform carrier frequency is decided to be 50Hz, the phase degree is 180 and the amplitude is 0.25V. The load resistor is set to 2KΩ in the CMOS rectifier circuit and the value of the internal resistance is obtained.

Three different design configurations are analyzed. The width size of PMOS and NMOS is set to be similar and varied from 4µm to 1100µm. For the first design configuration, the width size of transistor is 4µm. In the second design configurations, the width size is varied up to 750µm and third design configurations; the width size of transistor is varied up to 1100µm. This analysis is done to observe the variation of output voltage and overcome the voltage drop. A CMOS rectifier using 0.35µm technology was implemented using Microwind/DSCH Tool software.

Figure 2 shows the output current and voltage waveforms of the CMOS circuit from the simulation taken using 1100µm. From figure follow the change of the size of the PMOS and NMOS transistor, as the width size increase, the voltage drop on the resistor will less and internal resistance will become small. Hence this will increase the output voltage V_{OUT}. In Figure 2 shows that when the width size of the PMOS and NMOS transistors is w = 1100µm, output voltage = 1.20V, but when the width size of the MOS transistor is w = 750µm, output voltage = 0.61V. Therefore as the width size of the MOS transistor increases, the voltage drop on the whole will decrease and the value of output voltage is relatively high.

Figure 1(b): Voltage, Current vs Time when w = 1100µm

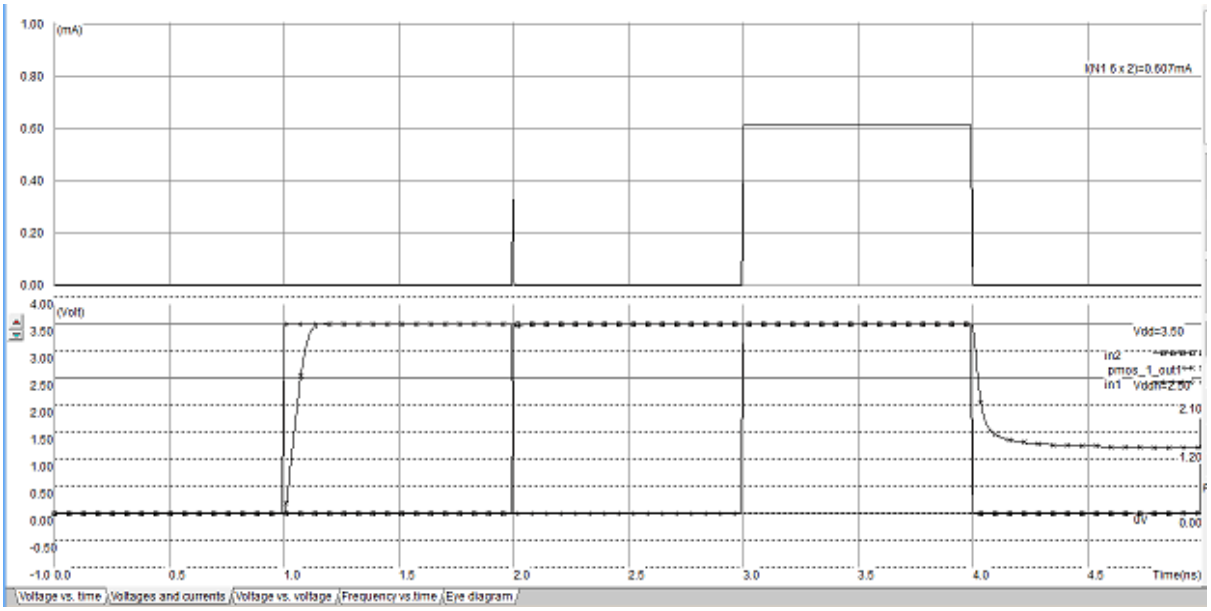

Table 2. Total Internal resistance at 1100µm width size

Paper	Width Size	Internal Resistance
Base Paper	1100µm	5.80Ω
Proposed Paper	1100µm	4.580Ω

Table 2.Represents the difference between the internal resistances obtained from the base paper and proposed paper at a constant width size about 1100µm. In the base paper, the internal resistance is 5.80Ω at 1100µm width size of PMOS transistor. The proposed work has less internal resistance at the 1100µm width size of the transistor.

5. CONCLUSION & FUTURE SCOPE

Based on the analysis the paper has proposed a very less voltage drop from the variation in the width size of transistor and minimization of the internal resistance in the CMOS rectifier. The simulation results is to determine the low Voltage drop and reduce internal resistance in CMOS rectifier. The variation in the width size of the transistors will affect the internal resistance and output voltage drop on the performance of the CMOS rectifier. By using 1100µm of width gives better output voltage which is 1.20V as compared to 750µm width which has 0.61V. The smaller width size of the transistor resulted in the large voltage drop in CMOS rectifier. An increase in the width size of the transistor is reducing the voltage drop. Since it has optimum output performance and low internal resistance, A future aspect will be focused on the best circuit design in CMOS rectifier design.

6. ACKNOWLEDGEMENT

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Himshikha Sharma has received her B.Tech degree in Electronics and Communication Engineering from Alpine Institute of Technology, Ujjain (M.P.). At present she is pursuing M.Tech in VLSI Design and Embedded System. Her area of interest includes low power VLSI design, Embedded systems.

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