Design and Performance Analysis of Reversible RSG Gate using QCA

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ABSTRACT
Quantum Dot Cellular automata employs the transistor less technology which overcomes the constraint of Moore's Law i.e. in forthcoming time the number of transistor affixed on a single chip cannot be increased further as it will reduce the performance of any circuit. A Reversible logic can contribute to the designing as it has many advantages over conventional circuits such as no forfeit of profitable information, low power utilization designs, win back of input from the output. In today's world each Nano-meter matters for the betterment of designs. In this paper, the improvement in the area of Reversible gates has been proposed so that the circuit could be more compact and efficient.

Keywords
Ancilla bit, Garbage Output, Hardware complexity, Quantum Cost, Delay, Multi-functionality, Reversible logic, Quantum computing.

1. INTRODUCTION
The term 'Reversible Logic' can be defined as retrieving the inputs from the outputs. This can be perceived by an example of normal life like melting of an ice cube. The input (water) can be regained from the output (ice). However, in irreversible logic [7] the input cannot be win-back from the output like we cannot regain milk (input) from curd (output).

The mandatory conditions for the reversible logic are as follows:

1) There should be equal number of inputs and outputs
2) No close path should be there
3) It should be a single-valued function

The Reversible logic [4] can be proved as an asset for the fields such as DNA computing, quantum computing, Optical processing of information, etc. It has gained lot of intentness because it surmount the flaw of irreversible logic i.e. heat dissipation [8] due to the deprivation of information.

1.1 Incentive for Reversible Logic
With the requirements, the circuits are becoming more intricate. Due to this, large numbers of transistors are implemented on small areas which restrict the performance of the circuit. To overcome this, there is a necessity of a logic that has many advantages like

1) Due to reversible computing [12] the speed would be increased, hence the efficiency
2) Reversible computing helps in reducing the size manifold, so the circuit would be more compact, hence easily portable
3) Cost effective and higher performance

2. TERMINOLOGY RELATED TO REVERSIBLE GATE

a) **Ancilla Bit:**
To make the number of input and output equal, extra pins are added in input side to fulfil the condition of reversibility. It can be either 0 or 1.

b) **Garbage Output:**
To maintain the reversibility, when the extra pins are added to the output side then it is called as garbage output [14].

c) **Hardware Complexity:**
The total number of basic logic operations like AND, OR and EX-OR performed in a circuit is defined as hardware complexity [6].

d) **Quantum Cost:**
The total number of basic logic gates used in a circuit to perform a specific task or operation is defined as quantum cost [7].

e) **Reversible Logic:**
It states that a unique output vector can be deduced from the input vector i.e. one to one mapping.

f) **Delay:**
The maximal amount of logic gates in the path between the input and its related output is measured in terms of delay.

g) **Multi-Functionality:**
Numerous functions can be performed by the logic gates by keeping one or more inputs invariable. This property of logic gates is known as multi-functionality [2].

h) **Input/ Output Count:**
The number of inputs and outputs present in the design is called I/O count.

3. PRIMARY REVERSIBLE LOGIC GATES

a. **Feynman Gate:**
It is also known as Controlled Not [10]. It has I/O count of 2 and Quantum cost of 1. It is represented by:
Input: A, B
Output: P, Q
Logic: P=A and $Q = A \oplus B = A\bar{B} + \bar{A}B$

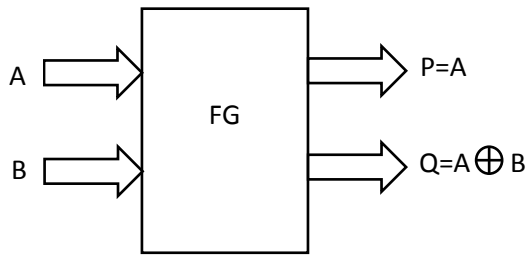Block Diagram is shown in Figure 1:

Figure 1: Feynman Gate

b. Toffoli Gate:

Toffoli gate [9] has I/O count of 3 and Quantum Cost of 5. It is represented as:

Input:	A, B, C
Output:	P, Q, R
Logic:	P=A
	Q=B
	R=AB$\bigoplus$C= (AB) $\overline{C}$ + $(\overline{AB})$ C

Block Diagram is shown in Figure 2:

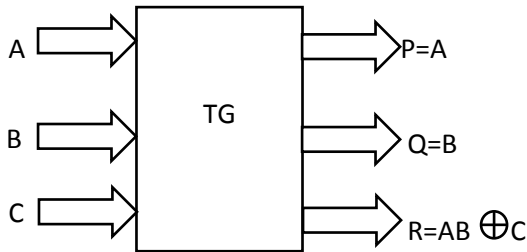**Figure 2: Toffoli Gate**

c. Peres Gate:

Peres gate [5] has I/O output count of 3 and Quantum Cost of 4. It is represented by:

Input:	A, B, C
Output:	P, Q, R
Logic:	P=A
	Q=A$\bigoplus$B = A$\overline{B}$ + $\overline{A}$B
	R=AB$\bigoplus$C = (AB)$\overline{C}$ + $(\overline{AB})$ C

Block Diagram is shown in Figure 3:
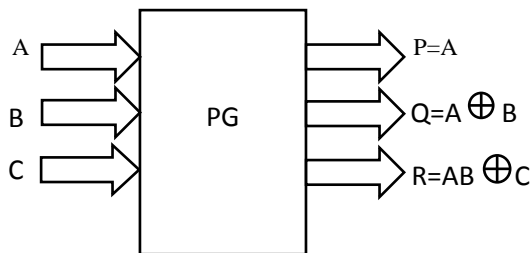
Figure 3: Peres Gate

d. FRG Gate:

FRG gate [11] has I/O count of 3 and Quantum Cost of 5. It is represented by:

Input:	A, B, C
Output:	P, Q, R
Logic:	P=A
	Q= $\overline{A}$B$\bigoplus$AC=($\overline{A}$B)$(\overline{AC})$+(AC)$(\overline{\overline{A}B})$

$R= \overline{A}C\bigoplus AB=(\overline{A}C)(\overline{AB})+(AB)(\overline{A}C)$
Block Diagram is shown in Figure 4:
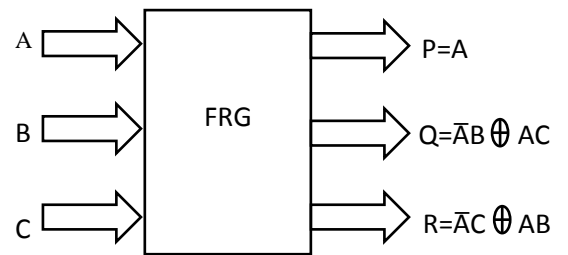
Figure 4: FRG Gate

e. NFT Gate:

NFT gate [3] has I/O count of 3 and Quantum Cost of 6. It is represented by:

Input:	A, B, C
Output:	P, Q, R
Logic:	P=A$\bigoplus$B
	Q=A$\overline{C}$$\bigoplus$$\overline{B}$C=(A$\overline{C}$)$(\overline{\overline{B}C})$+($\overline{B}$C)$(\overline{A\overline{C}})$
	R=A$\overline{C}$$\bigoplus$BC=(A$\overline{C}$)$(\overline{BC})$+(BC)(A$\overline{C}$)

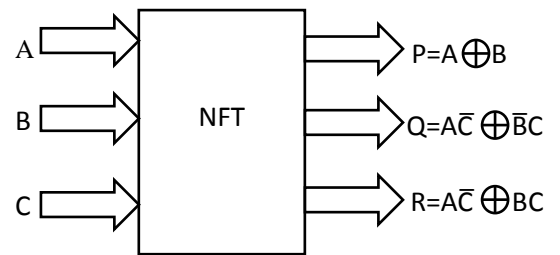Block Diagram is shown in Figure 5:

Figure 5: NFT Gate

f. RSG Gate

RSG gate [1] has I/O count of 3 and Quantum Cost of 5. It has highest multi-functionality among all reversible logic gates and most importantly its Garbage output is 0.

Input:	A, B, C
Output:	P, Q, R
Logic:	P=A$\bigoplus$ B
	Q=AB$\bigoplus$ C=(AB)($\overline{C}$)+(C)$(\overline{AB})$

$R=\overline{A}B\bigoplus C=(\overline{A}B)(\overline{C})+(C)(\overline{A}B)$

Block Diagram:
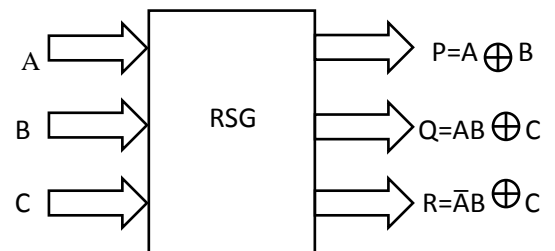
Figure 6: RSG Gate

Table 1: Truth Table of RSG

| C	B	A	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	1

Table 1 shows the truth table of RSG gates having A, B and C as inputs and P, Q and R as outputs. There is unique output pattern for respective input pattern.

4. PROPOSED WORK

This paper mainly emphasis on the area reduction in the designs of reversible gates available in the literature. As QCA works on the area reduction, therefore the compact circuits will definitely improve the functionality and efficiency.

4.1 Design layout of Feynman Gate

The QCA [13] implementation of Feynman Gate is shown in Figure 6. Design layout of FG using QCA is shown in Figure 6(a) and respective result is shown in Figure 6(b). The inputs (yellow) are indicated by A and B and outputs (blue) are indicated by P and Q.
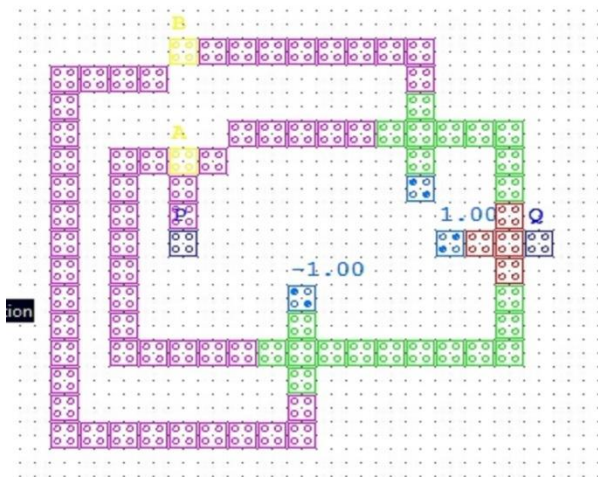
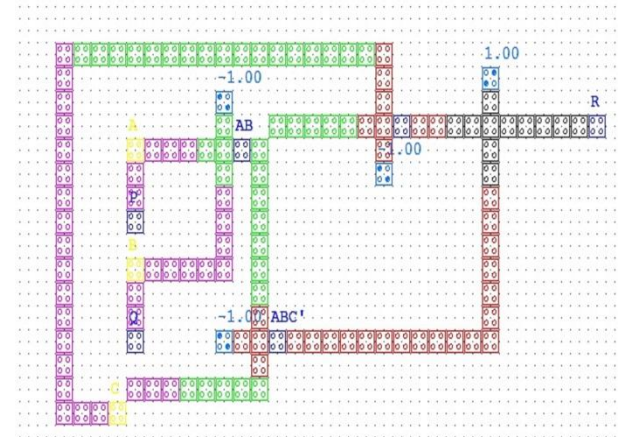**(a) Design Layout of FG using QCA**
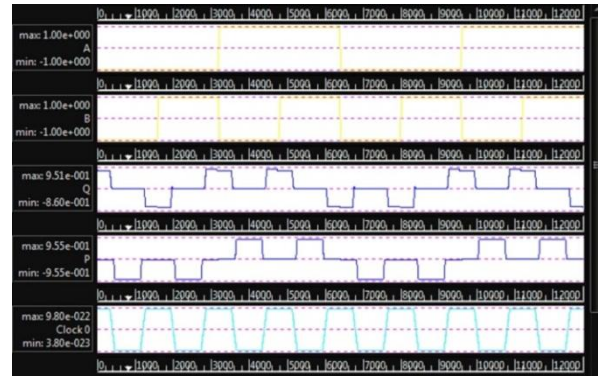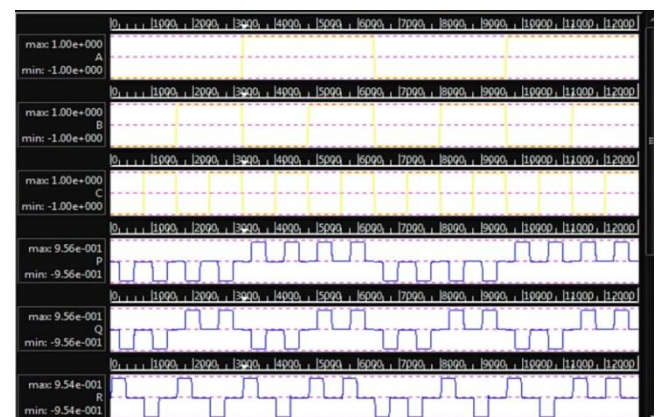

(b)Result waveforms

Figure 6: QCA Implementation of FG

4.2 Design layout of Toffoli Gate

The QCA implementation of Toffoli Gate is shown in Figure 7. Design layout of TG using QCA is shown in Figure 7(a) and respective result is shown in Figure 7(b). The inputs (yellow) are indicated by A, B and C and outputs (blue) are indicated by P, Q and R.

(a) Design Layout of TG using QCA

(b) Result Waveforms

Figure 7: QCA Implementation of TG

4.3 Design layout of RSG Gate

The QCA implementation of RSG Gate is shown in Figure 8. Design layout of RSG using QCA is shown in Figure 8(a) and respective result is shown in Figure 8(b). The inputs (yellow) are indicated by A, B and C and outputs (blue) are indicated by P, Q and R.
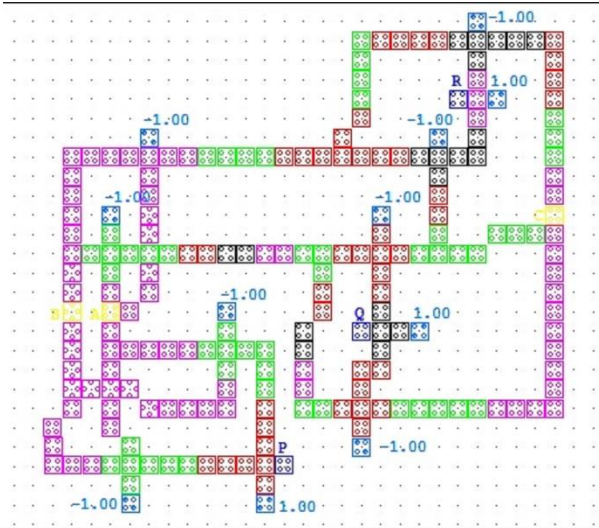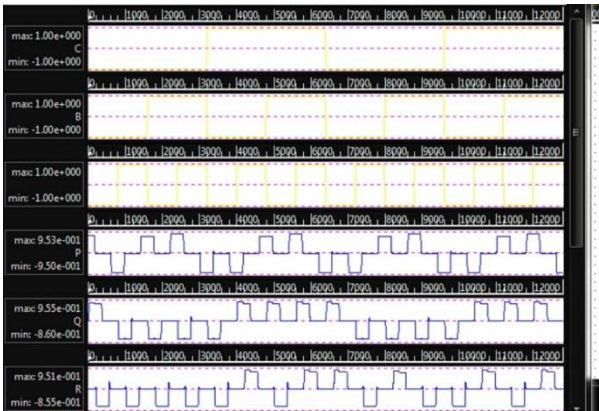
(a) Design Layout of RSG using QCA

(b) Result Waveforms

Figure 8: QCA Implementation of RSG

5. RESULT AND ANALYSIS

A comparative analysis among various Reversible Gates is shown in terms of multi-functionality below:

Table 2: Multi-functionality of Various Reversible Gates

Gate	NOR	OR	NOT	AND	NAND	XOR	XNOR	PASS	HA	HS	Operation counts
TG	X	X	X	✔	✔	✔	X	✔	X	X	4
PG	X	X	✔	✔	✔	✔	X	✔	✔	X	6
FRG	X	✔	X	✔	X	X	X	✔	X	✔	4
NFT	X	✔	✔	✔	✔	✔	X	✔	X	X	6
TR	X	X	✔	✔	X	✔	✔	✔	X	✔	6
RSG	X	X	✔	✔	✔	✔	✔	✔	✔	✔	8

Table 2 shows that RSG Gate has maximum number of operation counts.

Hereby a comparison between the area of existing reversible gates and revised reversible gates is shown below:

Table 3: Comparison of Reversible Gates in term of Area

Gate	Existing Gate Area $(\mu m)^2$	Revised gate Area $(\mu m)^2$	Per-cent improvement in Area
RSG	1.49	0.26	82.19
TG	0.31	0.20	35.48
FG	0.15	0.11	26.66

Table 3 shows the comparison of RSG, TG and FG present in literature and proposed design in terms of area $(\mu m)^2$.

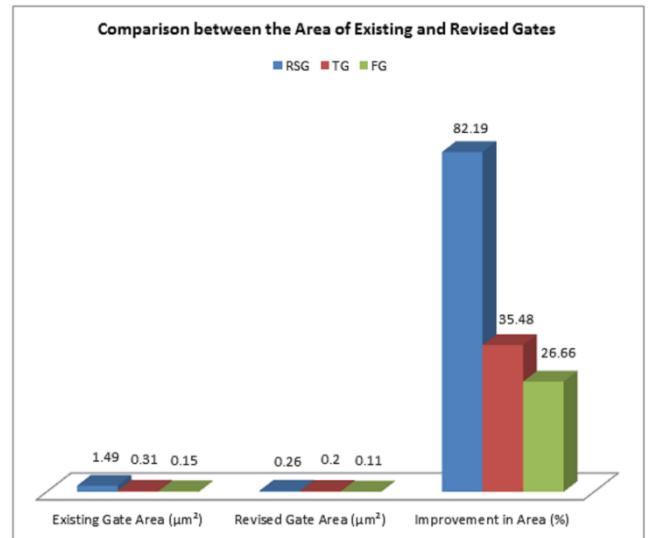The comparison is shown in the form of Bar Chart in Figure 9.

Figure 9: Comparison on the Basis of Area

Figure 9 shows the percent improvement in the area between already existing Reversible Gates and Revised Designs of Gates. The blue Bar indicates RSG gate with the area improvement of 82.18 percent, Red Bar indicates TG with the area improvement of 35.48 percent and Green Bar represents FG with area improvement of 26.66 percent.

6. CONCLUSION

In this paper comparison of existing designs and proposed designs of RSG, TG and FG is shown in terms of area. Since reversible gates perform manifold operations as compare to other irreversible gates, the improvement in the area can lead to an additional advantage to these gates. Due to the improvement in the area, the circuit would be more compact and hence would be more portable. As the area of the reversible gates has been improved, the speed of the circuit will definitely increase and the circuit will be more efficient. As it is known that, less will be the quantum Cost i.e. number of quantum gates, lesser will be the heat dissipation and loss of information. This would be beneficial in terms of performance of any circuit or device.

7. REFERENCES

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