Design and Simulation of OTA using DTMOS Technique in 180 nm CMOS Process

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ABSTRACT
In this paper, a low voltage low power CMOS Operational transconductance amplifier using DTMOS technique is described. The OTA is designed and simulated with 0.18µm CMOS technology. Simulation results show that with DTMOS technique, the open loop gain is 23.05 dB, the unity gain bandwidth is 379.7 KHz, phase margin is 93.8 degree, power consumption is 1.397 µw and input noise is 25.71 nv^2/Hz at 1 Hz frequency while operating at 0.6 v supply voltage and under 1 pF capacitor load. DTMOS technique provide low noise compared to conventional OTA. So DTMOS technique is suitable for low noise and low power applications such as biomedical applications.

Keywords
DTMOS, OTA, open loop gain, unity gain bandwidth, phase margin.

1. INTRODUCTION
In the past few years due to rapid growth of market for portable devices such as cell phones, portable computers and biomedical devices, design low power and low voltage analog integrated circuits with high performance has become an extremely important issue now a day's. The most common approach for decreasing power consumption is voltage supply scaling down. Because delivered power is proportional to the square of supply voltage according equation (1).

$$P = C_L V_{dd}^2 f_d \quad (1)$$

Since power supply reduction below $3V_t$ will degrade circuit speed significantly, scaling down the voltage supply should be accompanied by decreasing threshold voltage [1]. However, there is a lower limit for threshold voltage that is determined by amount of off state leakage current that can be tolerated. To surmount this problem, dynamic threshold voltage MOSFET (DTMOS) was proposed by F.Assaderaghi et al in 1994, which has highest V_t at zero and below zero bias and lowest value at $V_{gs}=V_{dd}$ [2],[3]. This dynamism in threshold voltage has been caused, DTMOS technique became most suitable for low voltage, low power application.

2. DTMOS TECHNIQUE
In DTMOS technique, the bulk is tied to its own gate as shown in fig. 1. The DTMOS technique reduces the transistor off state leakage current and also reduces the threshold voltage as transistor is on state ($V_{BS}>0$) according to equation (2).

$$v_{th} = v_{th0} + \gamma\left(\sqrt{|2\varphi_f - v_{BS}|} - \sqrt{|2\varphi_f|}\right) \quad (2)$$

Where v_{BS} is the source bulk voltage, v_{th0} is the threshold voltage as $v_{BS}=0$, γ is body effect factor with an approximate value between 0.3 to $0.4\sqrt{v}$, and φ_f is fermi potential with a typical value in range of 0.3 to 0.4 v [6].

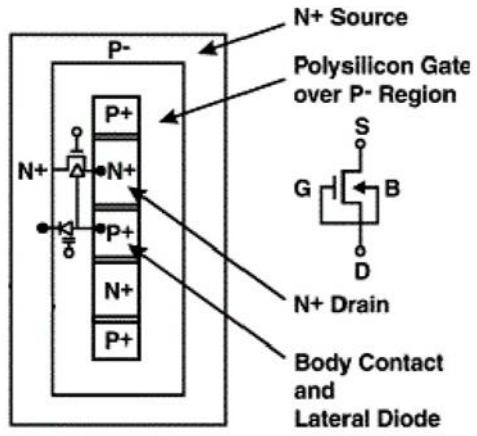

Fig 1: Dynamic threshold MOSFET [4]

3. PROPOSED OTA
The operational transconductance amplifier can be defined as an amplifier where all nodes are low impedance except the input and output nodes [5]. A simple example of a two stages OTA with fully differential pair and current mirror load is shown in Fig. 2. Where the first stage is combined differential pair two NMOS M_1 and M_2 with DTMOS technique as input and MOSFETs M_3 and M_4 as active load. DC gain small signal of OTA is given by equation (3):

$$A_v = g_{m2}(r_{o2} \parallel r_{o4})g_{m6}(r_{o6} \parallel r_{o8}) \quad (3)$$

MOSFETs $M_{3,7}$, $M_{4,8}$ and $M_{5,6}$ are current mirror. As seen Fig.2 due to symmetric of circuit, it is named as balanced OTA.

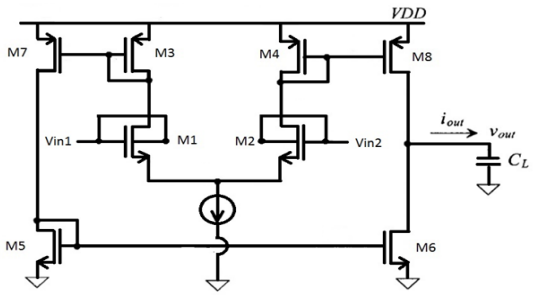

Fig 2: Figure of OTA with DTMOS technique

4. SIMULATION RESULTS
The simulation of proposed OTA has been performed with HSPICE in 0.18µm CMOS standard technology under 1pF capacitor load, 2µA constant current source and 0.6v power supply. Ratio W/L of MOSFETs is shown in table 1. Some of

feature of proposed OTA such as power consumption, open loop gain, phase margin, unity gain bandwidth and slew rate have been measured. Simulation results for AC analysis for open loop gain and phase is shown in Fig. 3 and Fig. 4 respectively.

Table 1. W/L Ratio

MOSFET	W/L
M1	500n/1u
M2	500n/1u
M3	3u/1u
M4	3u/1u
M5	240n/1u
M6	240n/1u
M7	500n/1u
M8	500n/1u

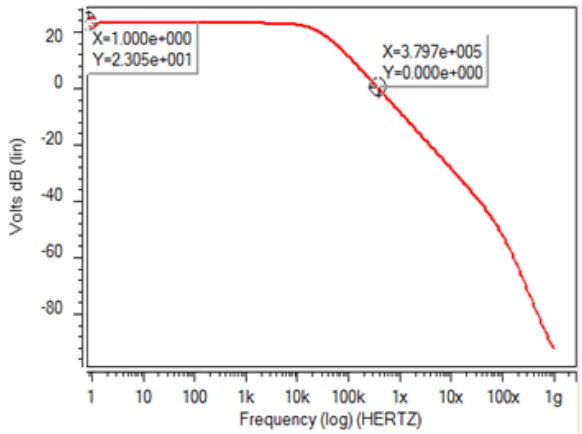

Fig 3: Simulated open loop gain with DTMOS

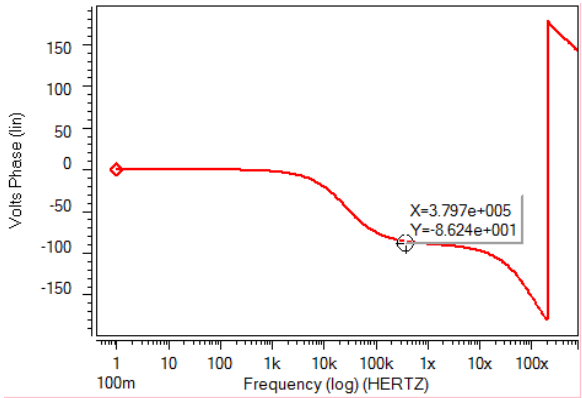

Fig 4: Simulated phase margin with DTMOS

With DTMOS technique, open loop gain is 23.05 dB, unity gain bandwidth is 379.7 KHz and phase margin is 93.8 degree. Without DTMOS technique, proposed OTA has 21.69 dB open loop gain, 325.3 KHz unity gain bandwidth and 94.5 degree phase margin. The slew rate value of OTA with DTMOS technique is shown in Fig.5 and is equal to 55 v/ms. Without DTMOS, the value of slew rate is equal to 49 v/ms.

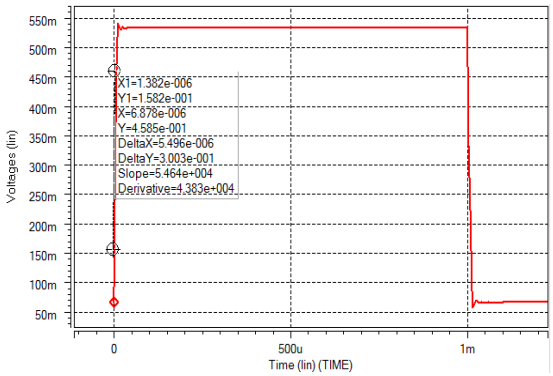

Fig 5: Simulated Slew rate with DTMOS

The simulated input voltage noise performance of the circuit is shown in Fig. 6. With DTMOS technique, the input noise is 25.71 nv^2/Hz at 1 Hz and 204.2 pv^2/Hz at 100 Hz, without DTMOS technique, the input noise is 42.28 nv^2/Hz at 1 Hz and 341.8 pv^2/Hz at 100 Hz.

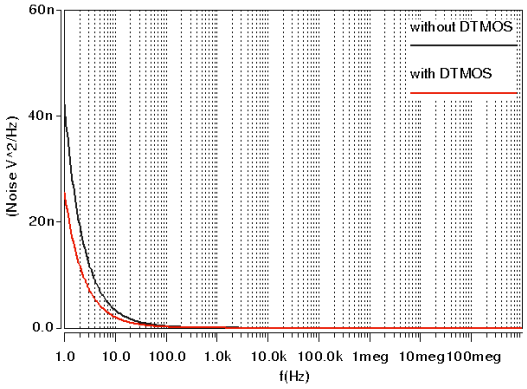

Fig 6: Simulated input noise

Table 2 shows a comparison with other low voltage low power operational amplifiers. To evaluate this work, figure of merit (FOM) is defined as equation (4) [8]:

$$FOM = \frac{Gain \times UGB}{Power\ Supply \times Power\ Consuption} \quad (4)$$

5. CONCLUSION

The design and simulation of low voltage low power operational transconductance with 0.18µm CMOS technology using DTMOS technique was performed. Simulation results show that with DTMOS technique, open loop gain is 23.05 dB, unity gain bandwidth is 379.3 KHz that in comparison with OTA without DTMOS technique has better results. Power consumption in both cases is approximately 1.397µw. because of the gate to body connection in DTMOS technique, the input noise is grounded and so it will be less in compared with conventional OTA as shown in Fig 6. Since using DTMOS technique has less input noise, this technique is suitable for low noise and low power integrated circuit design, especially for biomedical application.

Table 2. Comparison with other operational amplifier

	OTA	DTMOS OTA	[8]	[9]	[10]
Technology (µm)	0.18	0.18	0.18	0.18	0.18
Power Supply(v)	0.6	0.6	0.4	1	0.8
Power Consumption (µw)	1.397	1.397	0.386	33.1	100
Gain (dB)	21.69	23.05	91	60	56
UGB (kHz)	325.3	379.7	111	2730	3200
Phase Margin	94.5	93.8	66	62	45
Slew Rate (v/ms)	49	55	22	N/A	N/A
FOM (dB*kHz/mv* µw)	8.42	10.44	65.42	4.95	2.24

6. REFERENCES

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