Abstract

This paper includes User Defined Instruction Decoding using the Auxiliary Processor Unit (APU) controller which allows the designer to extend the native PowerPC 405 instruction set with custom instructions that are executed by an FPGA Fabric Co-processor Module (FCM) which accelerate the system performance with the APU Controller, with an aim that Portions of certain software applications that are implemented in software can run faster by moving the implementation into hardware. In a Virtex™-4 FX FPGA, the embedded PowerPC™ 405 (PPC405) processor can run software and offload computations to hardware modules in the FPGA. In such a system, a coprocessor interface known as the Auxiliary Processor Unit (APU)
Design of User Define Instruction Set using APU is used to transfer data between the processor and the FPGA. Because certain computations can be done more efficiently in software, and others in hardware, an APU-enhanced system results in a faster overall solution for many digital signal processing (DSP) applications.

References

- “Accelerated System Performance with the APU Controller and Xtreme DSP Slices”, xapp717 (v1.1.1) Sept. 29, 2005, @ www.xilinx.com.

Index Terms

Computer Science
And Sensor Network

Keywords

User Define Instruction, APU, FCM, Co-processor, Embedded Powerpc