Effect of Driver Width Variations on Propagation Delay of Driver-Interconnect-Load System

Evolution in Networks and Computer Communications
Journal
Number 2 - Article 4

Year of Publication: 2011

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Abstract
The performance of VLSI/ULSI chip is becoming less predictable as device dimensions shrinks below the sub-100-nm scale. Process variation is considered to be a major concern in the design of circuits including interconnect pipelines in current deep submicron regime. Process variation results in uncertainties of circuit performances such as propagation delay. The reduced predictability can be attributed to poor control of the physical features of devices and interconnects during the manufacturing process. Variations in these quantities maps to variations in the electrical behavior of circuits. The channel width of MOSFET varies due to changes in drain/source thickness; substrate, polysilicon and implant impurity level; and surface
charge. This paper provides a comprehensive analysis of the effect of channel width variation on the propagation delay through driver-interconnect-load (DIL) system. The impact of process induced driver width variations on propagation delay of the circuit is discussed for three different technologies i.e. 130nm, 70nm and 45nm. The comparison of results between these three technologies shows that as device size shrinks, the process variation issues becomes dominant during design cycle and subsequently increases the uncertainty of the delays.

**Reference**

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Automation Conference (DAC), 338–342.

Index Terms
Computer Science Communications

Key words
Process variation parasitic
propagation delay
driver width
load

technology node