Abstract

In current Deep Submicron (DSM) era, interconnects play important role in overall performance of the chip. The factors such as power dissipation and crosstalk through RC modeled interconnects substantially affect the entire working of the chip. Therefore, to enhance the performance, minimization or elimination of coupling between interconnects is essential. Bus-invert method is the best method which can simultaneously reduce coupling and power consumption of interconnects. The proposed method focuses on designing low complexity encoder for 4, 8 and 16 bit RC coupled lines. The encoder proposed occupies 37% lesser area than the most popular encoder. The power consumption of this encoder is 68% lesser and the
overall delay is also reduced by 57% compared to the existing encoders for RC modeled interconnects.

Reference


Index Terms

Computer Science
Communications
Design of Low Complexity Encoder for Capacitively Coupled VLSI Interconnects

Key words

Crosstalk
bus-invert
power
consumption
overall delay