Abstract

A low power pulse triggered flip flop (P-FF) design is done by the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. A conditional pulse enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse generation circuit can be reduced for power saving. Various post layout simulation results based on UMC CMOS 90-nm technology reveal that the enhanced pulse triggered FF design features the best power-delay-product performance in seven FF designs under comparison. Its maximum power
saving against rival designs is up to 38.4%. Compared with the conventional transmission gate based flipflop design. The average leakage power consumption is also reduced by a factor of 3.52.

References


Index Terms

Computer Science

Integrated Circuits

Keywords

Flip-flop  Low Power  Pulse Triggered