In this paper the design of a low power 10-bit segmented current steering DAC for instrumentation applications is presented. The static performance of segmented DAC depends upon the matching of current sources. The layout and switching scheme of current sources of the DAC is proposed to reduce the mismatch between the current sources for better accuracy and glitch while switching respectively. The prototype is fabricated in 0.35um two-poly three-metal CMOS technology and measurement results show maximum DNL of $+0.45/-0.326$ LSB and integral non-linearity INL of $+1.085/-0.7836$ LSB for 3.3v supply voltage. The total power consumption of the DAC is 3.39mW and core area of the DAC is 0.52mm².
Low Power 10-Bit Digital-to-Analog Converter in 0.35um Technology

References


Index Terms

Computer Science
Electronic Design And Signal Processing

Keywords
Dac  Inl  Dnl  Current Steering  Segmented Architecture