Abstract

The need for convolution and correlation arises most frequently in all signal processing applications, which demands for optimization in processing speed. In this paper an efficient architecture for the implementation of Fast Correlation and Convolution using FPGAs through DLX 32-bit RISC processor is proposed. The proposed methodology mainly focuses on the design of 32-bit pipelined RISC processor based on the DLX architecture to perform fast
convolution and correlation operations. The experimental results demonstrate that Field Programmable Gate Arrays FPGAs provide flexibility in architecture design and optimizes the processing speed in few nano seconds.

References

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Index Terms

Computer Science Electronic Design And Signal Processing

Keywords

Fpga Dsp Modelsim Correlation Convolution Spartan3 Xilinx