Abstract

A linear feedback shift register (LFSR) is proposed technique which targets to reduce the power consumption within BIST itself. It reduces the power consumption during testing of a Circuit Under Test (CUT) at two stages. At first stage, Control Logic (CL) makes the clocks of the switching units of the register inactive for a time period when output from them is going to be same as previous one and thus reducing unnecessary switching of the flip-flops. And at second stage, the LFSR reorders the test vectors by interchanging the bit with its next and closest neighbor bit. It keeps fault coverage capacity of the vectors unchanged but reduces the Total Hamming Distance (THD) so that there is reduction in power while shifting operation.
Power Reduction Technique in LFSR using Modified Control Logic for VLSI Circuit

References


- K. Paramasivam, "Reordering Algorithm For Minimizing Test Power In Vlsi Circuits"; Engineering Letter,
- K. Paramasivam, Dr. K. Gunavathi, "Reordering Algorithm For Minimizing Test Power In Vlsi Circuits"; Engineering 14:1, EL_14_1_15, February 2009.
Keywords
Built-in Self-test  VLSI Testing  Low-power Test Vector Pattern Generation