Reconfigurable Network on Chip Router for Image Processing Based Multiprocessor Applications

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Abstract

Real time Image processing (I.P.) systems, involving on board multiprocessor communication, use standard bus based communication. The load on the system to deliver the output towards real time standards call for high speeds, but for data intensive application such as IP algorithms require constant transfer of data between the logic cores. This would need either dedicated
connections or additional bus controllers. Networks-On-Chip (NoC) provide a structured way of realizing interconnections on silicon, and obviate the limitations of a bus-based solution. This paper deals with the design and implementation of a NoC router targeted for an Image processing system consisting of different modules. All the cores have been designed targeting real time frame rates. The design has been prototyped on a Virtex II FPGA. The timings are given in comparison to a standard DMA controller.

Reference


Index Terms

Computer Science
Information Technology
Key words

NoC

Virtex II

DMA

Router