Abstract

This paper presents a new pipelined architecture of Turbo decoder which runs at nearly four times the speed of a recently reported architecture with a reasonable increase in hardware. The proposed architecture is based on block-interleaved pipelining technique which enables the pipelining of the add-compare-select-offset (ACSO) kernels. Moreover next iteration initialization
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(NII) method has been adapted in the proposed work to initialize sliding window border values. The decoder chip consumes 219.8 mW of power at a maximum operating frequency of 192.3 MHz when implemented using 0.18 μm CMOS technology. Synthesis results indicate that the designed turbo decoder can achieve a decoding throughput of 38.46 Mb/s with an energy efficiency of 1.14 nJ/ bit/ iteration at the maximum operating frequency. The proposed architecture is therefore considered suitable for a real time wireless application such as video-telephony in mobile networks.

Reference

- Japan’s Proposal for Candidate Radio Transmission Technology on IMT-2000: W-CDMA

Index Terms

Computer Science

Information

Technology

Key words

Iterative turbo decoder

sliding window

high speed architecture

block interleaved pipelining

pipelined ACSO