Abstract

In this paper a technique is presented which improves the noise immunity of TSPC circuit. This technique is compared with other existing techniques. Analysis is carried out both for super and sub-threshold regions of operation. Investigations consider different performance criteria viz. noise immunity curve, power consumption, delay, average noise threshold energy (ANTE),
PANTE and DANTE. The new technique gives better results in the form of improved noise immunity of the TSPC logic. It is found that power dissipation is decreased by over three orders in sub-threshold regime. Scaled technology offers better noise immunity in sub-threshold regime. Simulation results are presented for 180nm technology node.

Reference

- BPTM for MOS model, http://ptm.asu.edu/
- Tanner EDA Tools,
Index Terms

Computer Science

Information

Technology

Key words

ANTE

DANTE

ANTE

TSPC circuit

Noise immunity

PANTE