Abstract

Power has become major design concern for complex VLSI circuits today. Designer needs tool(s) that accurately estimate the power dissipation in a given design. We need two categories of tools that are useful for this purpose. One is power optimization tools and, second is an analysis tool for estimating the power consumption in an existing netlist. This approach
addresses the second issue by employing a VERILOG-based approach for analysis of power consumption in CMOS logic designs. The design under test will either the result of logic synthesis with various optimization constraints or hand designs done through schematic capture. The proposed approach used to analyse various benchmark circuits for power consumption, such as ISCAS bench mark circuits. The presented approach in this paper consists of three phases: (1) Designing smart VERILOG simulation models, (2) Measuring transition activity at each node of the netlist and then estimate the power based on this activity and on fanout at each node, (3) Generation of smart input stimuli that achieve an upper bound in transition activity and hence power consumption. The estimates produced by this approach may provide useful feedback to designers or synthesis tools, allowing for better exploration of the design space.

Reference

- ISCAS bench mark circuits. www.eecs.umich.edu/~jhayes/iscas/-UnitedSataes


Index Terms

Computer Science

Information

Technology

Key words

Leakage power

Dynamic power
power dissipation

Bench mark

Verilog