Abstract

Propagation Delay of CMOS circuit depends upon several parameters such as threshold voltage, supply voltage, cell size. Variation of threshold voltage may result in temperature inversion effect thus reducing the cell delay as temperature increases. Integrated circuits operating at scaled supply voltage consume low power at the cost of reduced speed. This paper
presents the study of effect of temperature on propagation delay of LECTOR based NAND gate circuit and comparing that with conventional design for a temperature range of 25°C to 105°C.

**Reference**

- A. Dasdan and I. Hom. Handling inverted temperature dependence in static timing analysis. ACM Trans. on Design
Index Terms

Computer Science  Information

Technology

Key words

Leakage/Sub threshold current threshold voltage

LECTOR circuit