# Measurement of Oxide Thickness for MOS Devices, Using Simulation of SUPREM Simulator

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#### **ABSTRACT**

A procedure to characterize oxide thickness and conductor layers that are grown or deposited on semiconductor is by studying the characteristics of a MOS capacitor that is formed of the conductor - insulator - semiconductor layers. For a capacitor formed with oxide thickness of 510 Å (measured optically), here in this research author measures the oxide thickness by the SUPREM Simulator. Its accuracy depends on the quality of models, parameters and numerical techniques it employ. Authors also verify the result by measurment of capacitance at different voltages using LCR meter and the curve drawn through Visual Engineering Environment Programming (VEE Pro) software. Based on the oxide thickness measurement of a MOS capacitor, one can measure the device parameters, mainly the substrate dopant concentration and other parameter. This research was completed in BEL Laboratory.

#### Keywords

VEE Programming, Oxide thickness measurement, MOS devices, LCR meter, VLSI.

# 1. INTRODUCTION

The real importance of capacitance-voltage curve (C-V) measurement techniques in microelectronics field is that, a large number of device parameters can be extracted from two seemingly simple curves: high frequency C-V curve and quasistatic C-V curve. These parameters can provide critical device and process information.

We can divide the parameters into three groups.

- A). Includes typical MOS device parameters such as oxide thickness, flatband voltage, threshold voltage etc.
- B). Oxide charge parameters, includes interface trap charge density, mobile ion charge density etc.
  - C). Consists of doping-related parameters.

Also using C-t data, carrier generation lifetime and recombination lifetime can be extracted.

This research addresses the oxide thickness that can be extracted from a high-frequency C-V (HF-CV) curve. In this research authors first measures the oxide thickness using SUPREM programming and then proved that the thickness by using other method with the LCR meter and VEE Pro Software are same. Parameters of MOS device can be automatically calculated from data excel sheet at the end of the C-V test and then be automatically entered into the Data worksheet for the further test.

## 2. MEASUREMENT TECHNOLOGY

For the oxide thickness measurement, author fabricates MOS capacitors on a 4 inch diameter & 800 micron thick N-type silicon wafer and the grown layers were characterized by Capacitance - Voltage curve measurements.

#### 2.1. Fabrication of MOS Device

To fabricate metal-oxide-semiconductor, the silicon wafers were cleaned by following the standard cleaning procedure to remove insoluble organics and metallic contaminants. After that, a layer of oxide, approximately 500 Å thick, was grown on the silicon wafers using a dry oxidation process at 650°C for 60 minutes, with a pre-ramp of 5 °C per minute so that we reached at 950 °C and then a flat temp of 950 °C for the 110 minutes and at last postramp of 5 °C per minuts for 60 minutes with N<sub>2</sub> (12) & O<sub>2</sub> (32). All these process are shown in below programming of SUPREM. For top layer we will use Aluminum due to its ease of processing, ability to reduse native SiO<sub>2</sub>, which is always present in silicon wafers, exposed to atmosphere and its low resistivity. About 2000 Å of aluminium was then deposited over the oxide layer using a sputtering [2, 3].

Various techniques are used to increase the sputtering rates, use of magnetic field near the target to increase the generation of ions. Introduction of electrons by the use of an electron gun as a third electrode was also tried [4].

### 2.2. Introduction of SUPREM

SUPREM-III (Stanford University PRocess Engineering Model Version 0-83) is a computer program that allows the user to simulate the various processing steps used in the manufacturing of silicon integrated circuits or discrete devices. The types of processing steps, simulated by the current version of the program are inert ambient drive-in, oxidation of silicon and silicon nitride, ion implantation, epitaxial growth of silicon and low temperature deposition or etching of various materials. SUPREM-III simulates in one dimension, the changes in a semiconductor structure as a result of the various processing steps used in its manufacture [5].

The primary results of interest in this research are the thicknesses of the various layers of materials that make up the structure and the distribution of impurities within those layers. The program will also determine certain material properties such as polysilicon grain size and the sheet resistivity of diffused regions in silicon layers. A SUPREM-III structure may be doped with up to four impurities, with the default impurities being boron, phosphorus, arsenic and antimony.

#### 2.3. Simulation of SUPREM

To begin a SUPREM-III simulation, all of the coefficients and parameters for the materials and impurities must be input and the initial structure should be defined. Both of these functions are accomplished by the INITIALIZE statement.

In its simplest form the initial structure is a single layer of substrate material, though a more complicated multi-layer structure generated by a previous simulation may be specified. The coefficients are normally read from the default coefficient file and the structure may either be read from a previously saved structure file or defined through the parameters of the INITIALIZE statement. In the data file containing the input statements that control the SUPREM simulation, the INITIALIZE statement must precede all other statements except TITLE, COMMENT or STOP statements.

Once the coefficients and the initial structure have been defined, process simulation can begin as shown in Fig 1. If the user wishes to change any of the material or impurity coefficients, new values may be input by using the model parameter statements.

The coefficients defining the impurities are accessed through the impurity statements, BORON, PHOSPHORUS, ARSENIC, ANTIMONY and IMPURITY. The material coefficients are accessed through the SILICON, POLYSILICON, OXIDE, NITRIDE, ALUMINUM and MATERIAL statements. Other coefficients that apply to the interaction of materials and impurities may be controlled through the SEGREGATION (segregation coefficient), VOL.RATIO (voltage ratio) and MOBILITY statements. Oxidation rates are controlled by the parameters of the DRYO2 (dry O2), WETO2 (wet O2) and NITROGEN statements.

User can alters any of the coefficients, by using the SAVE FILE statement he may save the modified set of coefficients either into the default coefficient file, creating a new set of defaults.

#### 2.4. Measurement of Oxide Thickness

The results after the simulation of SUPREM are available in both printed and graphic forms which consist of all material and impurity coefficients as might have been specified by one or more of the MATERIAL, IMPURITY, SEGREGATION or VOL.RATIO statements, information about the current structure such as the thicknesses and composition of the various layers, impurity junction depths or resistivity of layers or diffused regions and the impurity concentrations at each node point and the distance of that point from the structure surface. Output consists of plots of the specified impurity concentrations versus distance as in Fig. 2 to 7.

```
Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.
E:\Documents and Settings\Administrator.USER-568BD47A70
E:\Documents and Settings>cd f:
E:\Documents and Settings>f:
F:\>cd viranjay
F:∖VIRANJAY>cd suprem
F:\UIRANJAY\SUPREM>suprem vii
    *** STANFORD UNIVERSITY
                                        ENGINEERING MODELS
                     * IBM PC/XT/AT * JFR UER1.09 *
ENTER INPUT FILE NAME:
ENTER OUTPUT FILE NAME:
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Figure 1. Simulation of SUPREM

# 3. CALCULATION OF OXIDE THICKNESS BY L-C-R METER

The fabricated capacitors electrically tested to characterize the material and to inspect the device performance. The variation of the capacitance (C) with gate voltage ( $V_G$ ) ranging from -5.0 Volts to +5.0 Volts and the capacitance with frequency ranging from 10 KHz to 1.2 MHz of a 100  $\mu$ m x 100  $\mu$ m capacitor are shown in Fig. 8. For the simplicity, author calculates the parameters for this curve.

Designed for measurement precision and ease of use, this family of E4980A L-C-R meter fits for both R&D and production applications. Although the LCR meter does not have all the sophisticated features as impedance analyzers, the LCR meter offers excellent performance at an affordable cost [6].

For a relatively thick oxide (>500 Å), extracting the oxide thickness is fairly simple. The oxide capacitance ( $C_{\rm OX}$ ) is the high-frequency capacitance when the device is biased for strong accumulation. In the strong accumulation region, the MOS capacitor (MOS-C) acts like a parallel plate capacitor and the oxide thickness may be calculated from  $C_{\rm ox}$  and the gate area using the following equation:

$$T_{ox} = A * \frac{\varepsilon_{ox}}{C_{ox}} \tag{1}$$

Here A is the gate area of metal =  $10^{-2}$  cm<sup>2</sup>,  $C_{ox} = 34.515*10^{-14}$  F-cm<sup>-1</sup>,  $C_{ox}$  is oxide capacitance measured by C-V curve for Accumulation region = 65 pF by Fig. 8, So after the calculation of (1), value of  $T_{ox}$  comes 510 Å.

So the capacitance measurement seems to be approximatly equal to actual value comes by the SUPREM simulation result [7, 8].

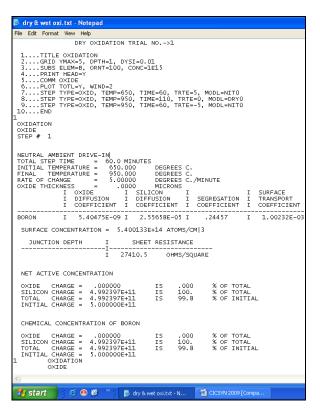


Figure 2. Programming and Drive-in of ambient

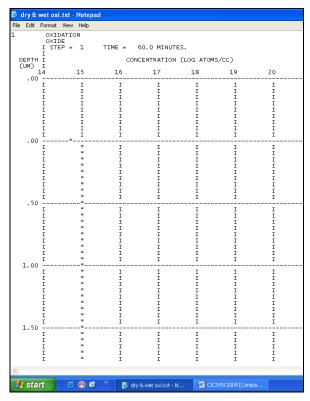


Figure 3. Curve for depth and concentration

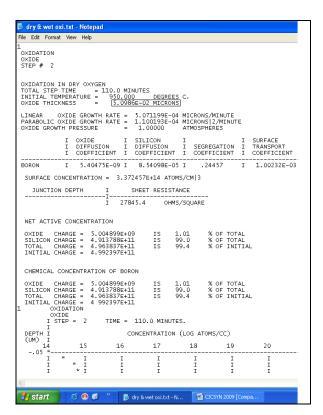


Figure 4. Oxide thickness measurements

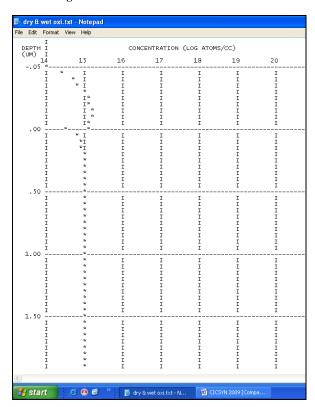


Figure 5. Curve for oxide thickness with concentration

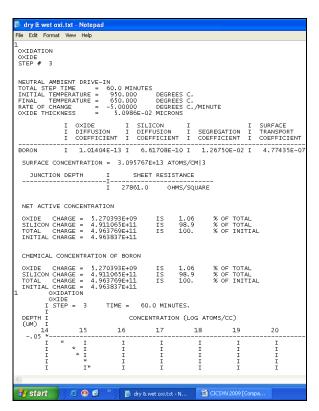


Figure 6. Natural Drive-in of ambient with sheet resistance

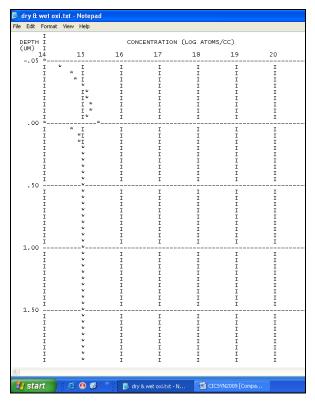


Figure 7. Curve for Drive-in ambient with concentration

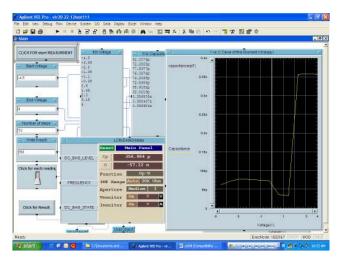


Figure 8. C-V curve at different voltages

#### 4. RESULT

Numerical simulations can be used optimize process recipes and test process sensitivity without costly and time-consuming experiments. Oxide thickness simulate by the SUPREM is equals to the thickness measured using LCR meter & VEE programming. Based on the oxide thickness measurement of a MOS capacitor with above process in BEL Laboratory, which resulted in errorfree values of oxide thickness, autor can measure the device parameters, mainly the substrate dopant concentration and other parameter [9, 10].

SUPREM can also be used to simulate oxidation using the Grove and Deal model and uses Arrhenius functions to describe the linear and parabolic rate coefficients for wet and dry oxidation. Oxidation processes are accessed using the same command as diffusion processes. SUPREM can calculate ion implant profiles and simulated impurities can be implanted, activated and diffused. This simulator can also handle implantation through multiple layers (i.e. through an oxide)

#### 5. CONCLUSION

The real importance of oxide thickness measurement techniques is that a large number of device parameters can be extracted from this result.

So we conclude that using this software we can get relevance data of the electronic devices. It can give faster result for calculation of parameters. Silvaco software version of SUPREM is SSUPREM3 (1-D) or SSUPREM4 (2-D) can be used for advanced applications. This experiment can be used for measuring it's cleaninig of pipes, furnaces & calibrate the parameters in fabrication Lab of a device. Except for a few simple cases, complications may arise in the calculation of diffusion and ion implantation profiles, and oxidation rates. Numerical methods have been developed to perform these computations in 1, 2 or 3 dimensions.

# 6. ACKNOWLEDGMENTS

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#### 7. REFERENCES

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