Improving the Power Quality by MLCI type DSTATCOM

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ABSTRACT

This paper proposes multilevel inverter type DSTATCOM for mitigating voltage sag at the load side. Cascaded H-bridge configuration for multilevel inverter with advanced phase shifted pulse width modulation technique is presented. Voltage sags are generated by faults the distribution feeder. First addresses with the three-phase 5-level cascaded multi level inverter and second addresses with the three-phase 7-level cascaded multi level inverter based on the shunt active power filter for mitigating the voltage disturbances. The proposed multilevel topology is simulated using MATLAB. The simulation results of the Fivelevel and Seven-level cascaded multilevel inverters are compared in different aspects.

Keywords

MLCI (Multilevel Cascaded Inverter), DSTATCOM Distribution static compensator, (VSC) Voltage Source Converter, THD (Total Harmonic Distortion) mitigation.

1. INTRODUCTION

Voltage sags are one of the most dominating power quality assets, which dragged the attention of many researchers as the sensitivity of loads are increasing due extensive usage of power electronic devices. Fault at distribution level, sudden increase of loads, motor starting are some of the causes of the voltage sags. Such sudden variations of voltage are undesirable for sensitive loads. These undesirable voltage sags can be mitigated by connecting controlled devices either in series or shunt to the load. A few of such devices are dynamic voltage restorer (DVR) and DSTATCOM (Distribution Static Compensator). Both these devices require voltage source converters to satisfactory operation. Many topologies have been proposed in recent past for voltage source converters.

Multilevel inverter has drawn attention of many researchers. There are three topologies of multilevel inverters-cascaded, flying capacitor and diode clamped, each having its own advantages in various applications. Cascaded H-Bridge multilevel inverter is one of the popular converter topologies used in high-powermedium-voltage (MV) drives. H-Bridge cascaded inverter [1] is one of the popularly used converter topology. The cascaded inverter type dynamic voltage restorer with neural control strategy is proposed [2]. The CHB inverter using 5-multilevel topology offers the following advantages.

- 1) Its structure will be simple and requires fewer components.
- 2) Simplicity of structure so the packaging layout is much easier.
- To reaches high voltage and reduce harmonics by their 3) own structure. Generates multistep staircase voltage waveform similar to pure sinusoidal output voltage by increasing the number of levels.

A new PWM-based control scheme has been implemented to control the electronic values in the two-level VSC used in the D-STATCOM [3-4] various control strategies have been proposed for voltage source PWM converters mainly [5-10] The Multilevel inverters require advanced PWM strategies like level shift, phaseshift or phase deposition. Among these PWM strategies phaseshifted PWM is described in this paper.

The paper is divided as per the following sections. Section-I gives the overview of the total project. Section-II presents the description of DSTATCOM. Modulation strategy is described in section-III. Section-IV & V depicts the description of the test system and simulation results. Finally conclusions are presented in section VI.

2. Shunt voltage controller DSTATCOM

The principle of shunt voltage controller is Fig1. The actual controller has the same configuration as the series controller. But instead of injecting the voltage difference between the load and the system, a current is injected which pushes up the voltage at the load terminals. The load voltage during the sag is the superposition of voltage due to the system and the voltage change due to controller. A DSTATCOM does not contain any active power storage and thus only injects or draws reactive power. Limited voltage sag mitigation is possible with the injection of reactive power, but active power is needed if both magnitude and phase angle of the pre-event voltage needs to be kept constant. A DSTATCOM consist of a Seven-level voltage source converter (VSC), an isolated dc energy sources and coupling transformer connected in shunt to the distribution network. The dc voltage across the storage device in to a set of three-phase ac output voltage by using VSC converters. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. A multifunction topology which can be drawn from VSC connected in shunt with the ac system.

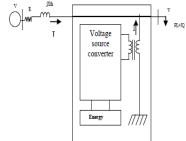


Fig 1: Schematic diagram of DSTATCOM

The multifunction topology can be achieved from VSC connected in shunt with the ac system which can be used for up to three quite distinct purposes.

- 1) Power factor correction
- 2) Current harmonics elimination

3) Voltage regulation and compensate of reactive power Fig-1 the shunt injected current I_{sh} corrects the voltage sag by adjusting the voltage drop across the system impedance Z_{th} . The value of I_{sh} can be controlled by adjusting the output voltage of the converter. The shunt injected current Ish can be written as

$$I_{sh}=I_{L}-I_{s}=I_{L}-\frac{V_{th}-V_{L}}{z_{th}}\dots\dots(1)$$
$$I_{sh} \neq \eta = I_{L} \neq -\theta - \frac{V_{th}}{Z_{th}} \neq \delta - \beta + \frac{V_{L}}{Z_{th}} \neq -\beta$$

The complex power injection of the DSTATCOM can be expressed as

$$S_{sh} = V_L I^* sh \dots (2)$$

In DSTATCOM the voltage sag correction depends on the value of Z_{th} (or) fault level of the load bus. The desired voltage correction can be achieved without injected any active power in to the system. When I_{sh} minimized, the same voltage correction can be achieved with minimum apparent power injection in to the system.

3. Controller

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load is connected, under system disturbances. The control system only measures the r.m.s voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the Fundamental Frequency Switching (FFS) methods favored in FACTS applications. Besides, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses. The controller input is an error signal obtained from the reference voltage and the value r.m.s of the terminal voltage measured. Such error is processed by a PI controller the output is the angle δ , which is provided to the PWM signal generator. It is important to note that in this case, indirectly controlled converter, there is active and reactive power exchange with the network simultaneously: an error signal is obtained by comparing the reference voltage with the r.m.s voltage measured at the load point. The PI controller process the error signal generates the required angle to drive the error to zero, i.e., the load r.m.s voltage is brought back to the reference voltage.

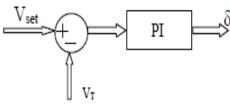


Fig 2: PI Controller for DSTATCOM

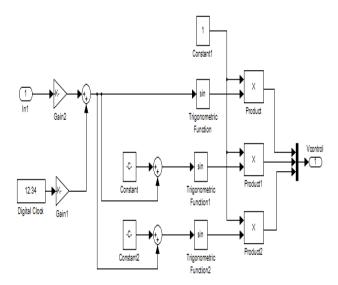


Fig 3: Generation of reference control signals for PWM controller

4. Modulation Strategy

Usually stair case modulation is commonly used for cascaded Hbridge converters. For SCM, the switching instants of each module are calculated offline to attenuate certain harmonics In that case dc link voltage has to be varied in accordance to the desired ac output voltage. Due to bulk dc link voltage dynamic response slows down. As the voltage sag duration ranges from half cycle to 30 cycles, fast dynamic response is required for the DSTATCOM application. Based on this consideration, Phase shifted PWM modulation scheme is adopted to maintain a relatively constant dc link voltage while achieving the fast dynamic response required of the output voltage by varying modulation index Multilevel inverters require carrier based modulation schemes due to higher levels. The carrier-based modulation schemes for multilevel inverters are classified as phase-shifted and level-shifted modulations. Multilevel inverter with m voltage levels requires (m-1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the peak-peak amplitude with phase shift between any two adjacent carrier waves given by

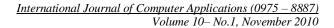
$$\phi_{CT} = \frac{360^{\circ}}{(m-1)}$$
 (3)

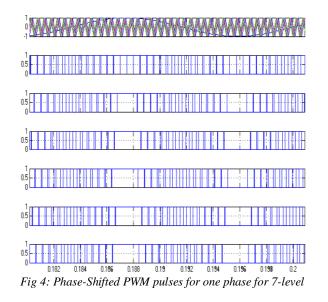
The sinusoidal signal V_{control} is phase-modulated by means of the angle α .

i.e.,
$$Va = \sin(\omega t + \delta)$$

 $Vb = \sin(\omega t + \delta - 2\pi/3)$
 $Vc = \sin(\omega t + \delta + 2\pi/3)$

The modulated signal Vcontrol is compared against a phase shifted triangular signals in order to generate the switching signals for the VSC valves. The Fig 4 shows the pulses for one phase for 7-level. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal, and the frequency modulation index of the triangular signal.





The amplitude index is kept fixed at 1 pu, in order to obtain the highest fundamental voltage component at the controller output.

$$M_a = \frac{V_{control}}{V_{tri}} = 1p.u \qquad (4)$$

Where Vcontrol is the peak amplitude of the control signal $V_{\rm tri}$ is the peak amplitude of the triangular signals. The switching frequency is set at 2000 Hz. The frequency modulation index is given by

$$Mf = fs/f1....(5)$$

Where flis the fundamental frequency

The modulating angle is applied to the PWM generators in phase A. The angles for phases B and C are shifted by 2400 and 1200, respectively. It can be seen in that the control implementation is kept very simple by using only voltage measurements as the feedback variable in the control scheme. The speed of response and robustness of the control scheme are clearly shown in the simulation results. The voltage level and switching state of the 7-level CHB (Cascaded H-bridge inverter) multi level inverter is as shown in the following tables.

Table 1. Voltage level & switching state of 7-level multilevel inverter

Output Voltage Van	Switching State								
	S11	S31	S12	S32	Vh1	Vh2			
3E	1	0	1	0	Е	2E			

2E 1 1 1 0 0 2E 0 0 1 0 0 2E E 1 0 1 1 E 0 1 0 0 0 E 0 0 1 1 0 E 0 0 0 1 1 0 E 2E 0 0 1 1 0 -E 2E 0 0 0 0 0 0 0 0 0 0 1 1 0 0 -E 1 1 0 0 0 0 -E 1 0 0 1 E -2E 0 1 1 1 1 E 0 -2E 1 1 0 1 0 -2E -2E 1 1 0 1 0 -2E -3E 0 1 0 1 -2E -2E							
E1011E01000E010110E2E00000000000000111000111000-E11110-E1001E011100-E1001E01002E-2E110100010-2E110100012E00010	2E	1	1	1	0	0	2E
Image: series of the series		0	0	1	0	0	2E
1 1 0 1 1 0 $-E$ $2E$ 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 1 1 1 0 0 0 1 1 1 0 0 0 $-E$ 1 0 0 1 E $-2E$ 0 1 1 1 1 $-E$ 0 $-2E$ 1 1 0 1 0 $-2E$ 0 0 0 1 0 $-2E$ 0 0 0 1 0 $-2E$	Е	1	0	1	1	Е	0
0000000000110011000001110000-E1001E-2E0111100-2E1100-E0-2E11010-2E0001012		1	0	0	0	Е	0
1 1 1 0 0 1 1 1 1 1 0 0 1 1 1 0 0 0 0 $-E$ 1 0 0 1 E $-2E$ 0 1 1 1 1 $-E$ 0 $-2E$ 0 1 0 0 $-E$ 0 $-2E$ 1 1 0 1 0 $-2E$ 0 0 0 1 0 $-2E$		0	1	1	0	-E	2E
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-E 1 0 0 1 E -2E 0 1 1 1 E -2E 0 1 1 1 -E 0 -2E 1 0 0 0 -E 0 -2E 1 1 0 1 0 -2E 0 0 0 0 1 0 -2E		1	1	0	0	0	0
0 1 1 -E 0 0 1 0 0 -E 0 -2E 1 1 0 1 0 -2E 0 0 0 1 0 -2E		1	1	1	1	0	0
0 1 0 0 -E 0 -2E 1 1 0 1 0 -2E 0 0 0 0 1 0 -2E	-Е	1	0	0	1	E	-2E
-2E 1 1 0 1 0 -2E 0 0 0 1 0 -2E		0	1	1	1	-E	0
0 0 0 1 0 -2E		0	1	0	0	-E	0
	-2E	1	1	0	1	0	-2E
-3E 0 1 0 1 -E -2E		0	0	0	1	0	-2E
	-3E	0	1	0	1	-E	-2E

5. Test system

Single line diagram of the test system for DSTATCOM is shown in Fig.5 and the test system employed to carry out the simulations for DSTATCOM is shown in Fig.6 Such system is composed by a 13 kV, 60Hz generation system, feeding two transmission lines through a 3-winding transformer connected in $Y/\Delta/\Delta$, 13/115/15 kV. Such transmission lines feed two distribution networks through two transformers connected in Δ/Y , 15/11 Kv.

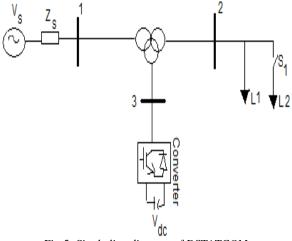


Fig 5: Single line diagram of DSTATCOM

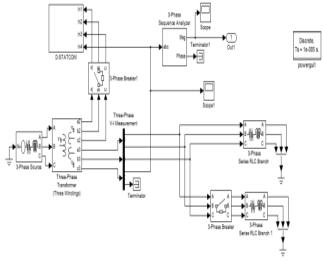


Fig 6: Simulink model of DSTATCOM

To verify the working of a DSTATCOM employed to avoid voltage sags during short-circuit, an additional load is switched on for 100msec. The capacity of the dc storage is 5KV. Using facilities available in MATLAB/SIMULINK the DSTSATCOM is simulated to be in operation only for the duration of the fault as it is expected to be the case in practical situation. Power System Bock set for the use with MATLAB/SIMULINK is based on state-variable analysis and employs either variable or fixed integration-step algorithms.

Fig.6 shows the simulink model of the test system for DSTATCOM.

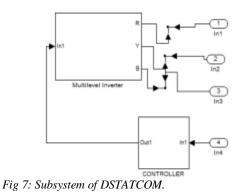
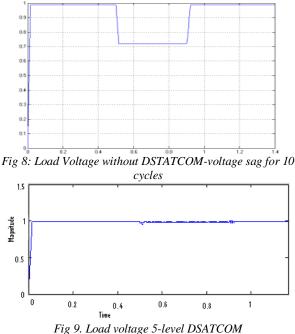


Fig.7 shows the subsystem of DSTATCOM. The reference control signals are generated considering the phase angle jump δ for 7-level MLI. The phase shifted pulse width modulation for single phase is shown in Fig.4.

6. Results

The first simulation contains no DSTATCOM and a single line to ground fault is applied at point A in Fig.8 via a fault resistance of $0.2\Box$, during the period 500900ms. The voltage sag at the load point is 30% with respect to the reference voltage. The second simulation is carried out using the same scenario as above but now with the DSTATCOM in operation. The total simulation period is 1400ms.



With isolated dc voltage of 5.87KV

When the 7-level (cascaded H-bridge inverter) DSTATCOM is in operation the voltage sag is mitigated almost completely, and r.m.s voltage at the sensitive load point is maintained at 98% as shown in Fig.9. The total harmonic distortion is maintained at 0.57% at the load end.

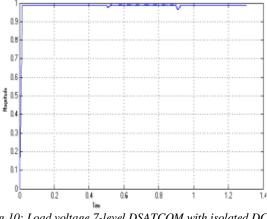


Fig 10: Load voltage 7-level DSATCOM with isolated DC of 3.25KV.

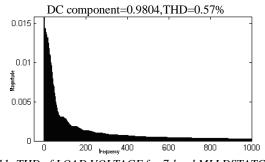


Fig 11: THD of LOAD VOLTAGE for 7-level MLI DSTATCOM

7. Conclusions

The cascaded 7-level inverter topology has been presented for shunt active power filter (DSTATCOM). The advanced pulse width modulation technique (PSPWM) is used for level inverter. The advantages of cascaded inverter in modeling of DSTATCOM are presented clearly. The THD in 7-level inverter is less compared to 5 level inverter, 7-level inverter. The following observations are made based on simulation results.

- 1) With cascaded multilevel inverter dc voltage requirement can be reduced, i.e. with low dc voltage higher ac voltages can be produced.
- 2) As dc voltage requirement is less, the proposed topology is more economical.
- 3) Filter at the output of the inverter can be eliminated with multilevel topology further reducing the cost of the filter.
- 4) The total harmonic distortion is well within the acceptable limits.

8. References

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