Power Optimized ALU for Efficient Datapath

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ABSTRACT
With the scaling of technology and the need for high performance and more functionality, power dissipation becomes a major bottleneck for microprocessor systems design. Also clock power can be significant in high performance systems. In this paper, a low power ALU for efficient datapath is proposed. In ALU, based on the observation, that while one functional unit is working other functional units remain idle, but they are connected to clock and all units dissipating significant amount of power. By using clock gating technique, a significant amount of power saving can be achieved at high frequency operations. Functionality of proposed ALU implemented on FPGA is tested using Xilinx tool. Power analysis is carried out using Xilinx's Xpower analysis tool. It is found that designed ALU is dissipating a power of 24mw when it is operated at a clock frequency of 15MHz and supply voltage of 2.4V under load current of 4.8mA

General Terms
Architecture, Low power.

Keywords
Clock Gating, ALU, Dynamic power, Microprocessor, Datapath, Simulation.

1. INTRODUCTION
Present day general purpose microprocessor [11] designs are faced with the daunting task of reducing power dissipation. Since power dissipation is becoming a bottleneck for future technologies, lowering power consumption is important for not only lengthening battery life in portable systems, but also improving reliability and reducing heat removal cost in high performance systems.

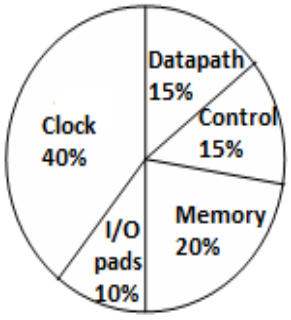


Figure 1. Power distribution in high-performance CPU

Figure 1 shows the power distribution among different units of a recent high-performance CPU. The clock is the largest power consuming component which includes clock generator, clock drivers, clock distribution tree, latches, and clock loading due to all the clocked elements. Out of these, clock loading shares bulk amount of power.

Large VLSI circuits such as processors [2] contain register files, arithmetic units and control logic. The register file is typically not accessed in each clock cycle. Similarly, in an arbitrary sequential circuit, the values of particular registers need not be updated in every clock cycle.

If simple conditions that determine the inaction of particular registers can be determined, then power reduction can be obtained by gating the clocks of these registers. When these conditions are satisfied, the switching activity within the registers is reduced to negligible levels. The same method can be applied to "turn off" or "power down" arithmetic units when these units are not in use in a particular clock cycle.

Clock power is the major component of microprocessor power [6], because the clock is fed to most of circuit blocks, including ALU. Arithmetic and logic units are the core of microprocessors where all computations are being performed. Demand for performance at low power in today's general purpose processors has put severe limitations on ALU design. ALUs are also one of the most power hungry sections in the processor's datapath [4][15] and are often the possible location of hot-spots.

Total power dissipation of chip consists of two components. 1. Static power dissipation which is due to leakage current of transistor during steady state and it is very small. 2. Dynamic power dissipation [10]. This has two components, (a) short circuit power dissipation which is a function of slew rate and by applying sharp clock edges, this power dissipation can be made very small, (b) charge/ discharge power dissipation which is given by $P = fC_L V_{dd} V_s$, where f is the frequency of the clock, C_L is the load capacitance, V_{dd} is the supply voltage and V_s the output swing. When output swings from 0 to V_{dd}, then $P = fC_L V^2_{dd}$. V_{dd} should not be reduced to a very low value since there are various problems associated with lowering the voltage in CMOS circuitry; the drivability of MOSFET will decrease, signal becomes smaller, and moreover increase in gate delay occurs when operating voltage is reduced to 2V or less. This component of power is of interest in the present study, as the other components are negligible.

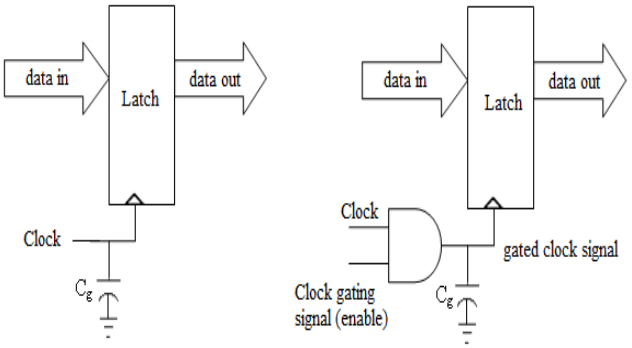
Reducing clock frequency affects the performance of the system. To reduce the power consumption without sacrificing the performance of the system, clock gating technique is used in the

proposed ALU architecture. The functionality of proposed architecture is verified using Xilinx and power is analyzed using Xpower power analysis tool.

2. CLOCK GATING

Dynamic power dissipation is the primary source of power consumption in CMOS circuits. This power dissipation occurs when changing input values cause their corresponding output values to change. Only small leakage currents exist as long as inputs are held constant. Clock gating [3][8][14] has been used to reduce power by disabling the clock on functional units [7][13] which are not connected. This approach can not only lower the switching activity at the function unit level, but also the switched capacitive load on the clock distribution network, there by reducing the power dissipation significantly. For these reasons, clock gating is currently viewed as one of the most effective logic, RTL and architectural power reduction techniques. In static CMOS circuits, disabling the clock on the latch that feeds the input operands to functional units essentially eliminates dynamic power dissipation. Power consumption on the critical clock lines is also saved because the latch itself is disabled. Currently most work on clock gating has focused on using the decoded opcode to decide which units can be disabled for a particular instruction.

Figure 2 (a) shows the schematic of latch element in which C_g is the latch's cumulative gate capacitance connected to the clock. As clock switches every cycle, C_g charges and discharges and consumes significant amount of power, even if the input do not change from one cycle to the next. In figure 2(b) the clock is gated by ANDing with control signal which is referred as clock gating (enable) signal. Here latch input is not required to change one clock cycle to another. Clock gating signal is turned off and clock is not allowed to charge/discharge C_g, hence saving clock power.



(a) **(b)**

Figure 2. Schematic of latch element (a) without and (b) with clock gating

3. PROPOSED ARCHITECTURE

The datapath elements are the functional blocks within a microprocessor that actually interact to perform computational operations. These tasks include reading from/writing to memory and register file, and arithmetic and logical operations. All microprocessors contain these elements in some form or the other, satisfying particular performance/price constraints. The block diagaram [5] of datapath shown in figure 3 captures the flow of data between components that operate on and store the data. The elements of a typical datapath are register file, ALU, RAM, multiplexer and decoder. The operands of the functional units come from several input registers: buffer, memory and general purpose register (GPR) file. The datapath writes back results to the output registers.

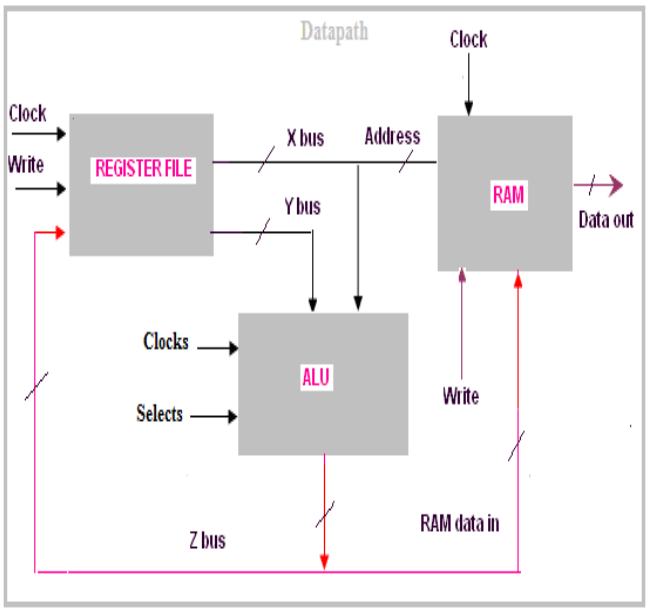


Figure 3. Block diagram of datapath

In the proposed work, 16 bit ALU of the datapath shown in figure 3 is considered, which performs eight arithmetic and eight logical operations selected by 4 bit code. Figure 4 shows inputs and outputs of ALU. Instead of designing ALU as a single module, it is divided into four functional blocks, namely, ARTH_1, ARTH_2, LOGICAL_1 and LOGICAL_2.

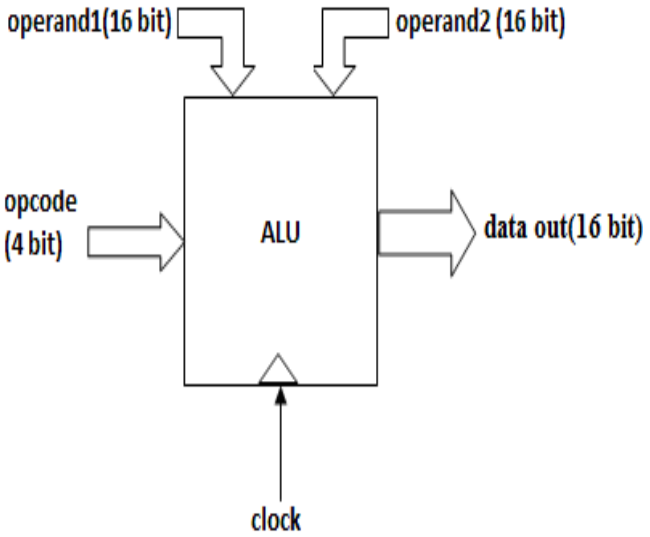


Figure 4. Proposed ALU module

Each block performs four different operations as shown in the functional Table 1. ALU takes 16 bit operands as inputs, process the operand data and gives 16 bit output data.

Table 1. Functions of ALU

Opcode ($D_3D_2D_1D_0$)	Operation	Active block
0000	Addition	ARTH_1
0001	Subtraction	
0010	Increment	
0011	Decrement	
0100	Multiplication	ARTH_2
0101	Add with carry	
0110	Clear Reg	
0111	Set Reg	
1000	NOT	LOGICAL_1
1001	AND	
1010	OR	
1011	EXOR	
1100	Shift left	LOGICAL_2
1101	Shift Right	
1110	Rotate left	
1111	Rotate right	

Figure 5 shows clock distribution in proposed ALU in which clock signals are not directly connected to the functional units (FUs) of ALU section. Instead, clock signals are gated with coded signals and are fed to the desired functional units. For example, while ARTH_1 is performing operations, remaining functional blocks ARTH_2, LOGICAL_1 and LOGICAL_2 are not performing any operations, such that, clock signal is delivered only to ARTH_1 functional unit.

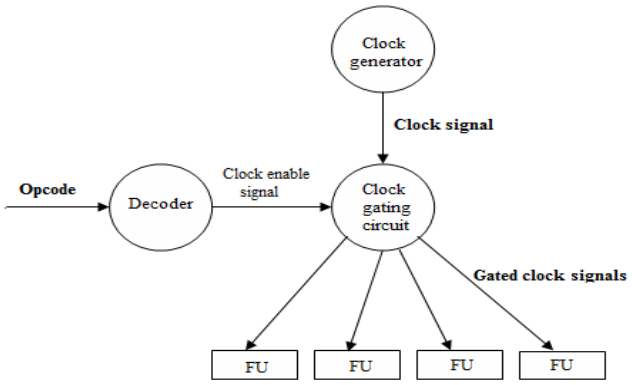


Figure 5. Clock distributions in proposed ALU

The internal architecture of ALU is shown in figure 6, which consists of a 2 to 4 decoder, clock gating circuit (array of AND gates), four functional units and one multiplexer. Decoder unit decode the opcode and generates clock enable signals, clock gating circuit generates gated clock signals to desired functional units, functional units [1] perform operations as given in Table 1, and multiplexer selects one of the functional unit outputs. Two out of four select lines are used to select the required operation. The proposed ALU operation can be explained as follows: D_3D_2 bits of the opcode selects one of the four AND gates as well as the required outputs of the functional units and D_1D_0 bits selects functional unit. For example, when opcode is "0100", 01 bits selects AND2 gate which in turn sends clock signal to the ARTH_2 unit, while for remaining units clock signals are not allowed. Bits 00 enables ARTH_2 unit to perform multiplication operation, the same bits/ lines used to select appropriate output from outputs of functional blocks with the help of MUX. Typically, the core of the ALU consists of functional units which take operands from register file, data cache or ALU write back bus [9]. The ALU output is multiplexed with the logical output through an output multiplexer.

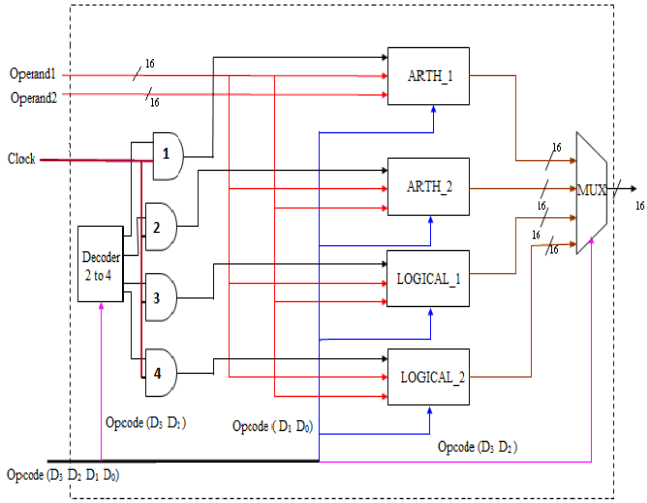


Figure 6. Internal architecture of proposed ALU

While ARTH_2 is performing operations remaining functional blocks ARTH_1, LOGICAL_1 and LOGICAL_2 are idle. As shown in figure 6, gated clock signals generated by the decoder controls the charge/discharge of the capacitance, C_g of the unused blocks thus saving clock power.

4. IMPLEMENTATION

Flow chart for clock gating circuit is shown in figure 7. Only when the clock event and clock enable signal occurs it allows clock signal to the required module.

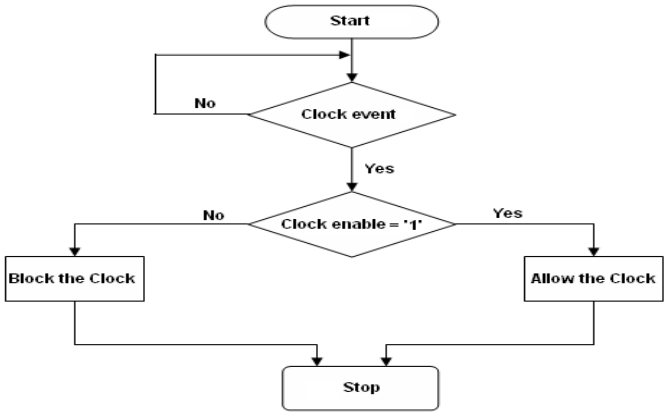


Figure 7. Flow chart for Clock gating circuit

The whole design is captured using VHDL language. The architecture of proposed ALU shown in figure 6 is implemented in different modules to get the desired functionality. The following steps are followed during implementation of this design: Code generation, Simulation, Synthesis, Power analysis, RTL schematic [12] and Technology schematic.

5. RESULTS

5.1 Simulation and Synthesis

The simulation results of ALU unit are presented in figure 8. The input signals are *aluoprand1(16 bit), aluoprand2(16 bit)* and the output signals are *alu_out(16 bit).* For example, when the opcode is "0100", it performs multiplication operation.

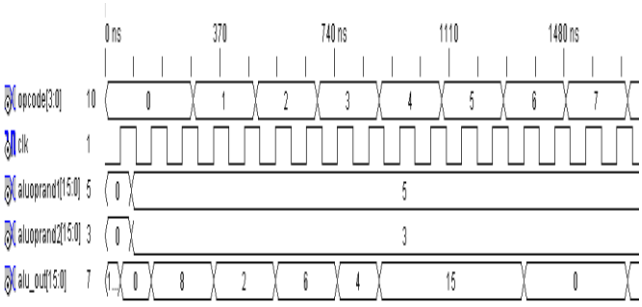


Figure 8. Simulation results of ALU

The RTL viewer of ALU is shown in figure 9. From this figure, it can be observed that the clock gating circuit controls the clock for different sections of ALU.

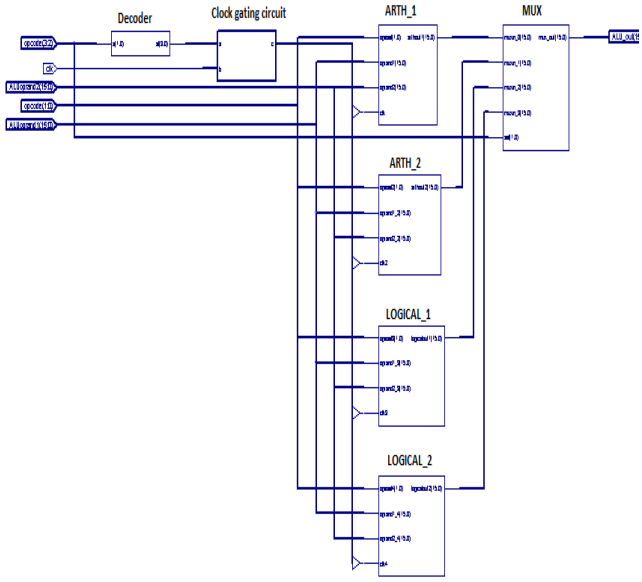


Figure 9. ALU RTL viewer

The Technogy viewer of ALU is shown in figure 10. This view shows a technology-level representation of ALU in terms of logic elements such as LUTs, carry logic, I/O buffers, and other technology-specific components - all HDL optimized to the target Xilinx device.

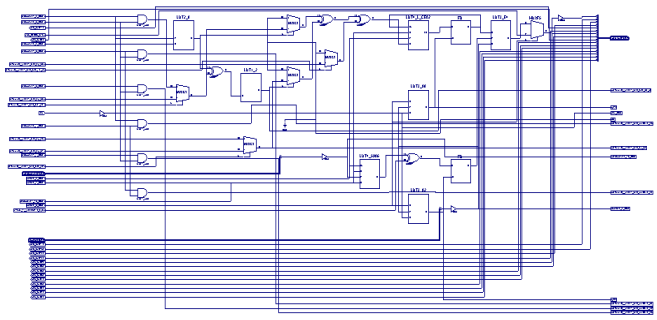


Figure 10. ALU Technology viewer

5.2 Power Analysis

Power analysis of low power ALU is carried out by using Xilinx's xpower analysis tool. Figure 11 shows variation of power dissipation with operating frequency for various supply voltages. It is observed that ALU is dissipating a power of 16mW at a frequency of 15MHz under no load conditions.

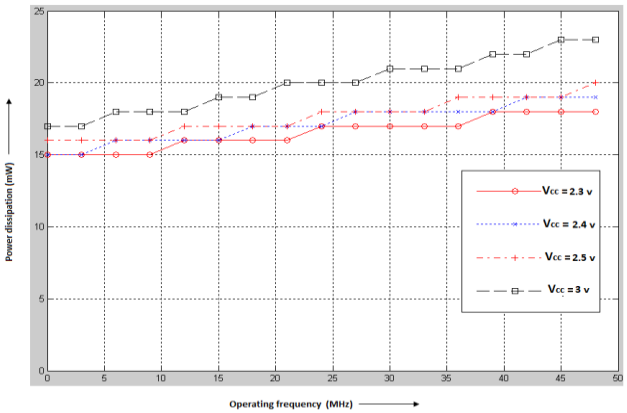


Figure 11. Variation of power dissipation with operating frequency for various supply voltages

Figure 12 shows the variation of power dissipation with load current for different operating frequencies and supply voltages. ALU is dissipating a power of 24 mW when it is operated at a clock frequency of 15 MHz and a supply voltage of 2.4V under load current of 4.8 mA.

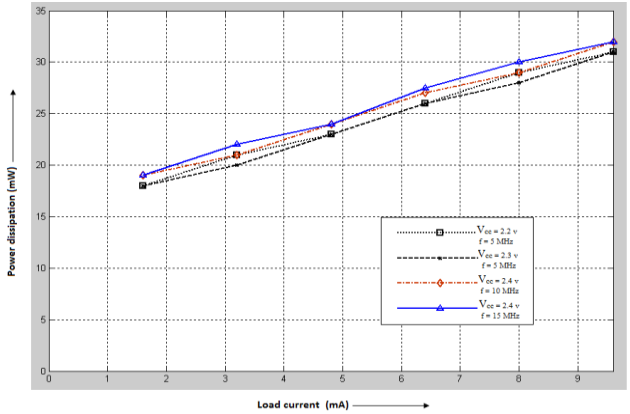


Figure 12. Variation of power dissipation with load current for different supply voltages and frequencies

5.3 Characteristics of ALU chip

Precision	16 bit
Architecture	low-power
Maximum Frequency (MHz)	281.770
Power Dissipation (mW)	24 *@15MHz*
Supply Voltage (V)	2.4
No. of functions	16
No. of pins	53

6. CONCLUSIONS

Power dissipation is becoming a limiting factor for high performance microprocessor design due to ever increasing device counts and clock rates**.** There are several approaches to reducing the power. In this work clock gating technique is applied to ALU to optimize the power. ALU is tested for different load conditions and supply voltages. It is found that it consumes a power of only 24mW @15MHz with a maximum frequency of 281.770MHz at a supply voltage of 2.4V under load current of 4.8mA. The designed chip can be used in the datapath design of microprocessor, RISC processor, or in any embedded system where ALU operations are required. This clock gating technique can be extended to whole system to achieve more power saving. One of the main challenges in future microprocessor design will center around devising new circuit techniques that help lower power without impacting overall circuit performance.

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