Voltage-Controlled Ring Oscillator for Low Phase Noise Application

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ABSTRACT
A design for a voltage-controlled ring oscillator (VCO) is presented. The design allows an implementation of low frequency ring oscillator using relatively small devices and less stage. It is implemented using .18um technology provided by TSMC technology using 3.3V power supply. The VCO topology exhibits a very wide tuning range from few Hz to 368.9 MHz. It also features the rapid voltage swing and the 48% duty cycle with good transient characteristics which is difficult to get from the conventional oscillator. Its power dissipation at the maximum oscillation frequency is 35.05 mW. A frame work for modeling the phase noise in complementary metal–oxide–semiconductor (CMOS) ring oscillators. Phase noise for simulated circuit is -88dbc when offset frequency is 10^5 HZ.

Keywords: ring oscillator, voltage controlled oscillator, inverter, transmission gate, phase noise

1. Introduction:
A voltage-controlled oscillator (VCO) is considered as one of the important building blocks in analog and digital circuits. [1],[2],[3]. For example, a VCO is the main building block in phase locked loop (PLL) and clock generator circuits in modern microcircuits, feeding clocks into chips must be avoided due to the effect of stray capacitance at the pins of IC package. High-speed circuits require on-chip oscillators to generate clocks. In recent years, LC oscillators [4] have been known with good phase noise performance, but their tuning range is relatively small (around 10-20%) and on-chip spiral inductors occupy a lot of chip area. On the other hand, ring oscillators usually have a wide tuning range, occupy less on-chip integration area, which makes them being more widely used than LC oscillators.

The design of a ring oscillator requires connecting odd number of inverters and feedback from the output of the last one to the input of the first one. Since the oscillation frequency is determined by the number of stages and the delay in each stage which is very small for an inverter, typically the achieved frequencies are several hundreds MHz to GHz in 0.18 μm technology. To achieve low frequency output, the number of stages has to be very large which is sometimes unacceptable.[5]. But the drawback of enlarging the driving capability is definitely to produce much power consumption. Another approach to achieving wide frequency range of the voltage-controlled ring oscillator is controlling the resistance. Compared to these methods above, it create the better chance to design a low power and wide tuning frequency range ring oscillator through the voltage-controlled resistor because it occupies small area and consumes no excess power consumption. The VCO given in this paper is suitable for wireless biotelemetry because of the low power and compact area. So the concern of low power becomes the key point of the requirement of the system.

2. CONVENTIONAL CIRCUIT
The conventional ring oscillator based VCO uses variable bias currents to control its oscillation frequency. However, when the bias current is quite small, the voltage swing of the VCO will become slower (longer rise/fall time). That is not desirable in some applications. In addition, increasing bias current will make the voltage headroom of the current source MOS transistors become narrow.[6].

A conventional voltage controlled ring oscillator circuit is shown in Fig.1 where N is an odd number and shows the number of inverter stages. Assume that the gate to source parasitic capacitances C_Gs of the NMOS and PMOS transistors are equal as is shown in Fig.2. Here the frequency of the oscillation can be found as

$$f_{osc} = \frac{1}{2N\tau} \quad (1)$$

Where τ is the delay of one inverter stage Using Fig.2, the delay of each inverter stage will be given

$$V_{osc} = \int \frac{I_{ctrl}}{C_G} dt \quad (2)$$

$$\tau = \frac{V_{osc} C_G}{I_{ctrl}} \quad (3)$$

Where Vosc is the oscillation amplitude. Substituting (3) into (1) will give

$$f_{osc} = \frac{I_{ctrl}}{2NV_{OSC}C_G} \quad (4)$$

Here the oscillation frequency is determined by the current Ictrl, the number of stages N, the amplitude V_{osc} and the parasitic capacitance C_G. For a given number of stages, the oscillation frequency can be controlled by varying control

current or amplitude only since C_G is a fixed parameter. control scheme by varying the current is commonly used.

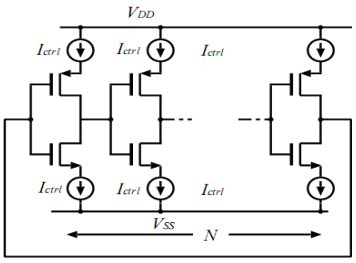

Figure1: Conventional voltage controlled ring oscillator.

Delay Circuit:

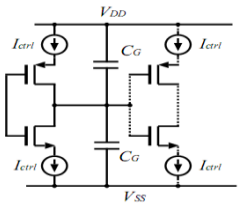

Figure2: Delay approximation

3. CHARACTERISTICS OF TRANSMISSION GATES

The transmission gate shown in Fig 3 is designed to act as a voltage-controlled switch. When V_G is high, both M_n and M_p are biased into conduction region and the switch is closed; at this time, the resistance of the transmission gate is very small. If V_G is low, then both MOSFETs are in cutoff region and the switch is performed like open circuit; In such case, we can consider the resistance of the transmission gate is ideally infinite. From above discussions, we can speculate that the resistance must vary greatly depending on the gate voltage. Shown in figure 4.

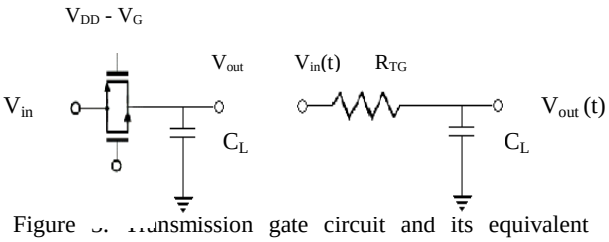

Figure 3. Transmission gate circuit and its equivalent small-signal RC model

4. BASIC CIRCUIT

The circuit scheme is shown in Fig.5. Here a variable resistor R_V is added at the input terminal of each inverter. The inverter itself is made from PMOS and NMOS

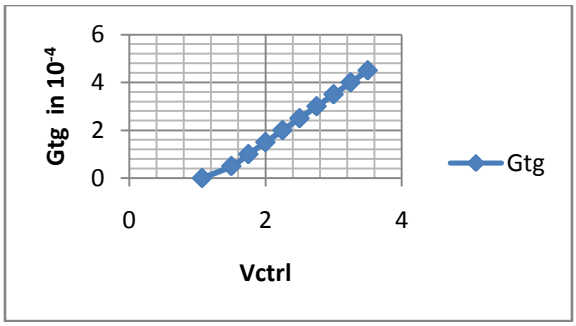

Figure 4. Gate voltage (V_{ctrl}) versus transconductance of ttansmission gate (Gtg)

transistors as is shown in Fig.6. The delay of each stage τ_p can be calculated from Fig.7. Since the MOS transistors in each inverter can be assumed as switches, it can be replaced by a resistance $1/G_M$ as is shown in Fig.5. If the transconductances G_Ms and parasitic capacitances C_Gs of NMOS and PMOS transistors are equal, the delay of each inverter stage τ_p then will be approximately

$$\tau_p = \frac{C_G(1 + G_M R_V)}{G_M} \qquad (5)$$

For a very large R_V such that $G_M R_V >> 1$,the delay will be determined by the time constant of R_V C_G regardless of the value of G_M. Assuming R_V =0 will give

$$\tau_p = \frac{C_G}{G_M} \qquad (6)$$

This is a delay for a simple inverter stage. Finally, the oscillation frequency can be found as

$$f_{osc} = \frac{G_M}{2NC_G(1 + G_M R_V)} \qquad (7)$$

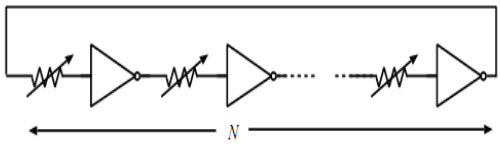

Figure5: voltage controlled ring oscillator.

Equation (7) shows that the oscillation frequency depends on the values of transconductance G_M , resistance R_V and capacitance C_G. However, G_M and C_G are device parameters and assumed to be constant. As a conclusion, the oscillation frequency can be controlled by changing the value of R_V .

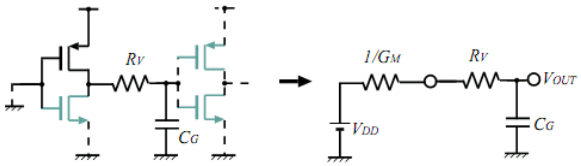

Figure6: Delay approximation of one stage

5. MODIFIED LINEAR MODEL FOR PHASE NOISE

In this section, we will derive the relation between the phase noise and the internal signal swing from a modified linear model for ring oscillators. We show that, in order to achieve phase noise comparable with that of the LC oscillators, fast transitions are needed, i.e. devices have to operate in a hard switching mode and be switched ON and OFF completely.

A. Theoretical Analysis

Fig.9 shows a simplified model for a three-stage ring oscillator. Each delay stage consists of a transmission gate and inverter. For this condition the single-side band (SSB) phase noise can be represented by (8) [7], where k is the Boltzmann's constant and T is the absolute temperature. The excess noise factor F accounts for the total noise from the passive resistor R and the active device -Gm [8]. Represents the peak-to-peak signal voltage, is the center frequency of oscillation, and is the offset from the center frequency

$$L(\Delta\omega) = \frac{32FkTR\Gamma_{rms}^2}{9}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \qquad (8)$$

Where Γ_{rms} is inpulse sensitivity function which is explained in appendix.

6. SIMULATION RESULTS

The simulation is performed using 0.18µm CMOS process parameters. Circuits used in the simulation are three-stage voltage controlled ring oscillators shown in Figs.8 and9. The W/L ratios of the MOS transistors are shown in Table1. The power supply V_{DD} for both circuits is 3.3V.

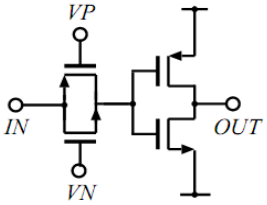

Figure7: Circuit implementation of the inverter circuit.

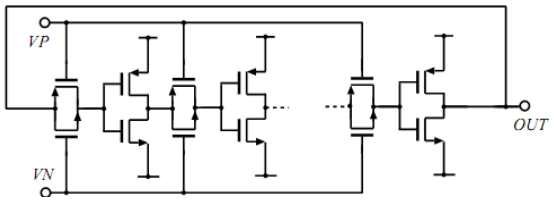

Figure8: Circuit implementation of the proposed Voltage controlled ring oscillator.

6.1 Transient Characteristics:

Fig.11shows the transient simulation result of the circuit when the control voltage is 1V. The oscillation frequency is 16MHz. Here the circuit has a faster voltage swing. In case of fosc =16MHz, the rise/fall time (10% ~ 90% of voltage swing) for the circuits are .186ns for oscillation frequency of 16MHz. Figure12 shows that how frequency is varying with $V_{ctrl.}$ simulation result of the current dissipation of the proposed circuit for fosc=16MHz is shown in figure 14. Here the circuit dissipates a large current in the transition of the output voltage of each inverter. As a result, the circuit has a faster voltage swing.

6.2 F-V Characteristic:

Simulation result of the f-v characteristic of the voltage controlled ring oscillator is shown in Fig.11, 12.The oscillation frequency for control voltage of 0.4V and 3V are 40Hz and 380MHz respectively. Here a frequency tuning range from tens of hertz to hundreds of megahertz is obtained. In addition implementation of low frequency oscillator using small size devices is also possible.

	W/L(um)
M_a	9/.6
M_b	3/.6
M_{sp}	1.35/.4
M_{sn}	.45/.4

Table 1. W/L ratio of inverter and transmission gate

7. CONCLUSIONS

A design of ring oscillator based VCO is simulated. The design allows implementation of a voltage controlled ring oscillator with wide tuning range and fast voltage swing. Simulation results show that the rise time/fall time of the circuit is .186n for oscillation frequency of 16MHz@1V. The circuit also achieves a tuning range from few Hz to 368.9MHz for control voltage between 0.4V to 3.3V. Furthermore, the maximum oscillation frequency of the circuit depends on the device parameter. Furthermore, the circuit is applicable for a low supply voltage because of its simple structure.

8. REFERENCES

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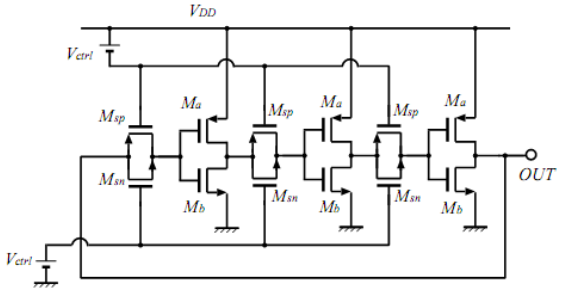

Figure.9: Circuit implementation of the simulated Voltage controlled ring oscillator.

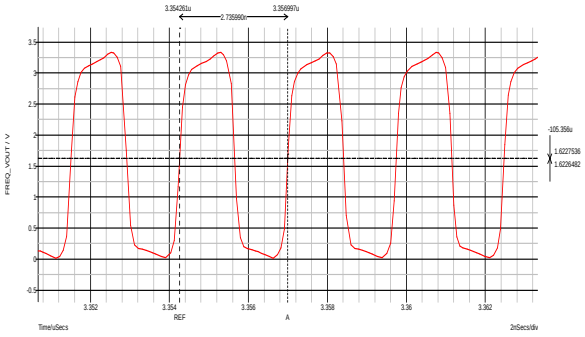

Figure10: Transient characteristic(f=368.9MHz) @3.3 V

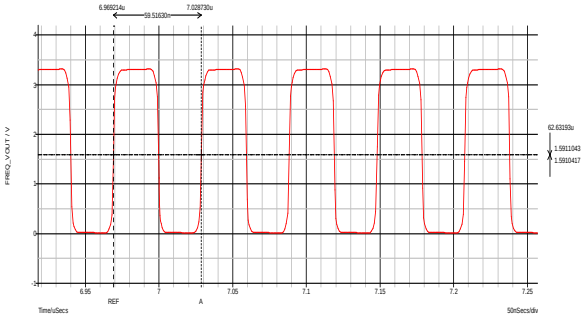

Figure11: Transient characteristic(f =16MHz) @ 1Volt

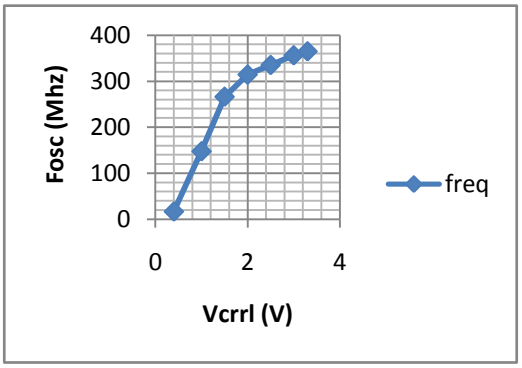

Figure12: F-V characteristic simulation results of the circuit.

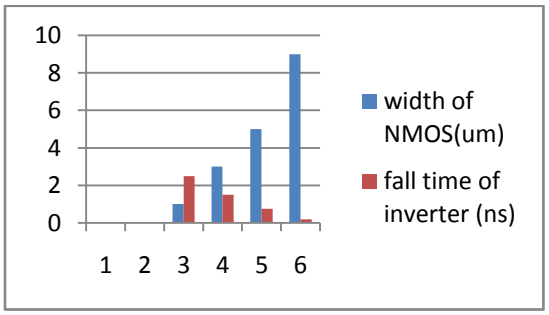

Figure 13:Rise time variation with variation of NMOS width

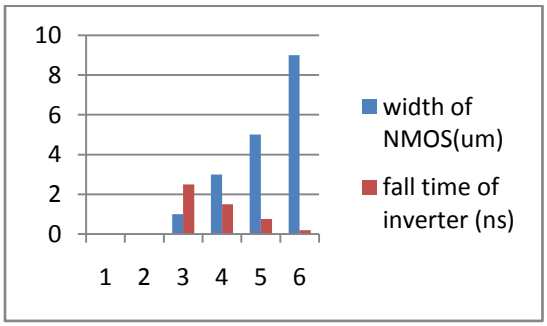

Figure 14: Fall time variation with the variation of the NMOS width

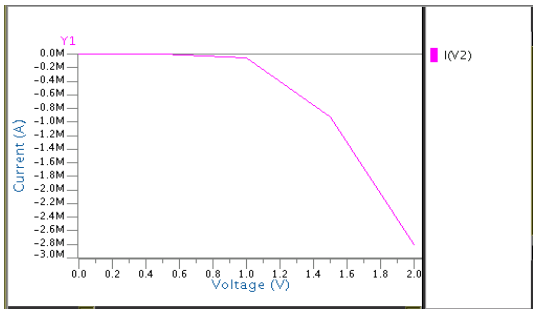

Figure13 DC Analysis voltage-current curve

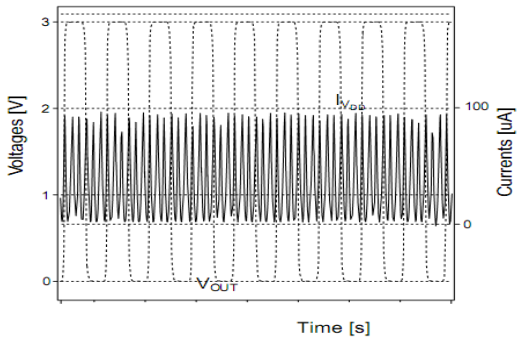

Figure 14 Current dissipation (fosc=6MHz)

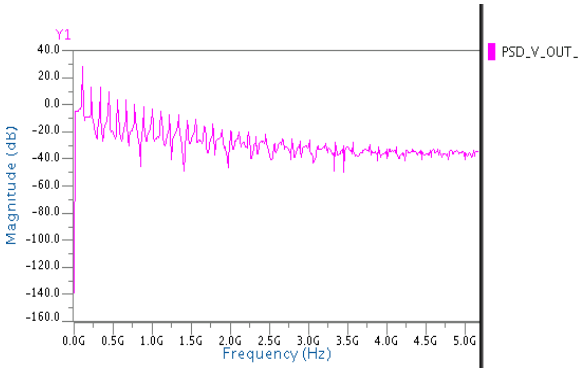

Figure 15 Power Spectral Density Vs Frequency

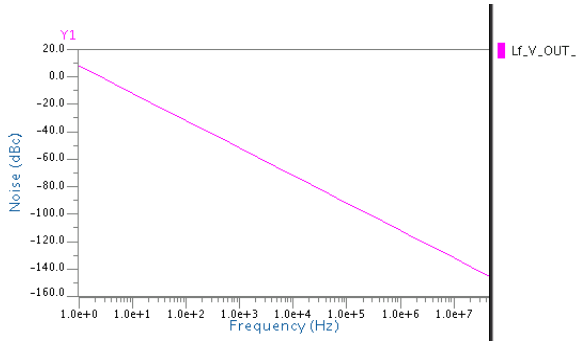

Figure 16 Phase Noise Vs Offset Frequency

9. MEASUREMENT VS SIMULATION RESULTS

	Theoritical	Simulation
Technology	.18um	
Power Supply	3.3V	
Max freq	370.1Mhz@3.3V	368.9Mhz
Min freq	3.9Mhz@1V	16Mhz
Power diss.	35.05mWatt	25.5mWatt
Phase Noise	-90dbc	-88dbc

Appendix

Calculation of the Impulse Sensitivity Function

In this two different methods to calculate the ISF. The first method is based on direct measurement of the impulse response and calculating from it. The second method is based on an analytical state-space approach to find the excess phase change caused by an impulse of current from the oscillation waveforms. The third method is an easy-to-use approximate method.

A. Direct Measurement of Impulse Response

In this method, an impulse is injected at different relative phases of the oscillation waveform and the oscillator simulated for a few cycles afterwards. By sweeping the impulse injection time across one cycle of the waveform and measuring the resulting time shift $\Delta t, h_{\phi}(t, \Gamma)$, can calculated $\Delta\emptyset = 2\pi\Delta t/T$ noting that ,where is the period of oscillation. Once $h_{\phi}(t, \Gamma)$ is found, the ISF is calculated by multiplication with q_{max} .This method is the most accurate of the two methods presented.

B. Calculation of ISF Based on the First Derivative

This method is actually a simplified version of the second approach. In certain cases, the denominator of (36) shows little variation, and can be approximated by a constant. In such a case, the ISF is simply proportional to the derivative of the waveform. A specific example is a ring oscillator with N identical stages. The denominator may then be approximated by f'^2_{max}

$$\Gamma_i(x) = \frac{f_i'(x)}{f'^2_{max}} \qquad (9)$$