FTL based 4Stage CLA Adder Design with Floating Gates

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ABSTRACT
Low-voltage and low-power circuit structures are substantive for almost all mobile electronic gadgets which generally have mixed mode circuit structures embedded with analog sub-sections. Using the reconfigurable logic of multi-input floating gate MOSFETs, 4-bit full adder has been designed for 1.1V operation. [1],[2] Multi-input floating gate (MIFG) transistors have been anticipating in realizing the increased functionality on a chip. A multi-input floating gate MOS transistor accepts multiple inputs signals, calculates the weighted sum of all input signals and then controls the ON and OFF states of the transistor. This enhances the transistor function to more than just switching. Implementing a design using multi-input floating gate MOSFETs brings down transistor count and number of interconnections. Here in this we have presented how to eliminate the propagate and generate signals this tends the design to become more efficient in area and power consumption by using feed through logic [8]. It has been included the four stage sum signal in FTL based adder with floating gates. The following information is about Carry look ahead adder circuit, tested with 45nm technology and is extended to ALU. The proposed circuit has been implemented in 45n-well CMOS technology.

Keywords
Mirror adder circuit, MIFG, FTL, CMOS adder.

1. INTRODUCTION
1.1 A floating gate transistor is a kind of transistor in which its driving terminal is electrically isolated from the rest of the device. [1], [2] Since there is no direct internal DC path from the input terminal to the other terminals, the resistance is high. The main advantages of the floating gate transistors are the high input resistance and the simplified driving characteristics of the device operating in voltage mode. The two important floating gate transistors are: the IGBT and the FGMOSFET**.**

1.2 A FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. [5],[6] A number of secondary gates or inputs are then deposited above the floating gate (FG) and are electrically isolated from it as shown in the Fig 1. These inputs are only capacitive connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node.

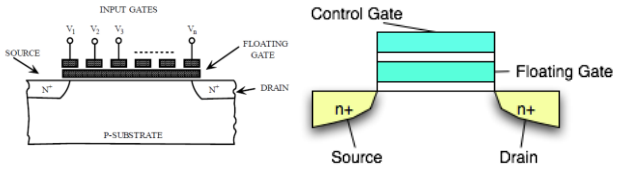

Fig 1: Floating gate structures

2. DEVICE CHARACTERISTICS
A floating-gate transistor in the simplest form is a standard MOS transistor with a capacitor in place of a gate contact. The device shown in Figure 2.a is an example of typical floating gate. Multiple coupling capacitors are often used in designing floating-gate transistors. The relationship between the terminal voltages and drain current of the two-input floating-gate is shown below.

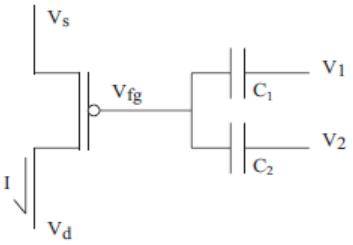

Fig 2.a: Multi input floating gate equivalent model

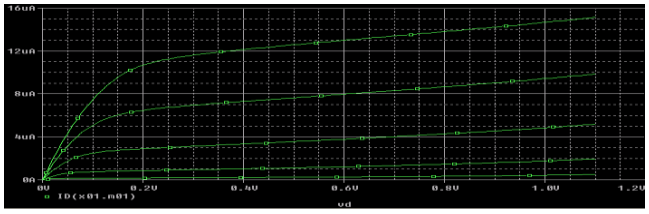

Fig 2.b: Multiinput floating gate and its characteristics.

Transistor, assuming saturated sub-threshold operation, is given by the following equation.

$$I = I_s e^{\frac{(V_{DD})-(Vdd-Vfg)}{Vt}} e^{\frac{V_D}{V_A}} \quad (1)$$

Where the floating-gate voltage is formulated by the following:

$$Vfg = \frac{1}{C_r}(V_1 + V_2 + V_3 ..... V_n) + V_W \alpha_W + V_{EQ} \quad (2)$$

Where

$$Cr = C1 + C2 + Cgs + Cgd \quad (3)$$

$\alpha_w = CW/CT$ is the coupling coefficient from the well input, *Vw*, to the floating gate. V_{EQ} is the equivalent voltages due to both the charges stored on the floating gate as well as the dc voltages at the source and drain that are capacitively coupled to the floating gate. There are at least two important implications of equation2: the gate voltage is a function of the charge stored on it, and the gate voltage is a function of any other voltage capacitive coupled to the gate. Because the gate voltage is a function of the charge stored on the floating-gate, the I-V curve of the transistor can be shifted to a particular, desirable point. Illustrated in Fig 2.b are a series of gate sweeps for a floating-gate device with different amounts of charge stored. The result is a single transistor with a wide array of possible effective threshold.

3. DESIGNING OF MAJORITY NOT FUNCTION BY USING FGMOS

Multiple-input floating gate CMOS inverter is shown in Fig. 5. V_1, V_2, V_3… V_n are input voltages and C_1, C_2, C_3… C_n are corresponding input capacitors. Equation 3 is used to determine voltage on the floating gate of the inverter. Weighted sum of all inputs is performed at the gate and is converted into a multiple-valued input voltage, Vin at the floating gate. [5]The switching of the floating gate CMOS inverter depends on whether Vin obtained from the weighted sum, is greater than or less than the inverter threshold voltage or inverter switching voltage (Vin). The switching voltage is computed from the voltage transfer characteristics of a standard CMOS inverter.

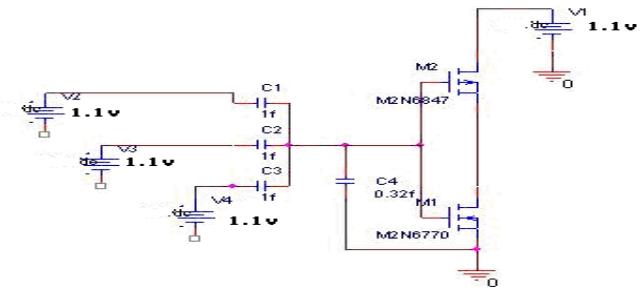

Fig 3: Three input CMOS inverter for carry generation of full adder

As shown in the above Fig 3 three input CMOS inverter is constructed. Majority NOT gate or majority NOR gates can be constructed using the above circuits .Here the problem is with delays associated with the circuits that can be adjusted by the proper logic effort.

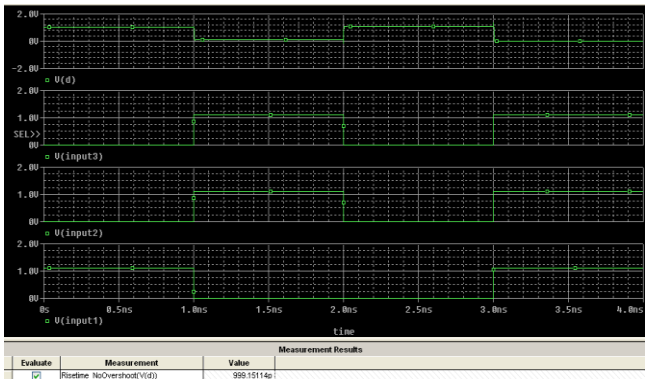

Fig 4: Carry output using MIFG CMOS inverter

4. PROPOSED METHODOLOGY

The main contribution of this paper is to introduce the new logic called multi input floating gate by using feed through logic in order to achieve the high performance carry look ahead adder for the embedded applications. FTL is a new logic derived from pseudo NMOS as shown in the Fig 5.

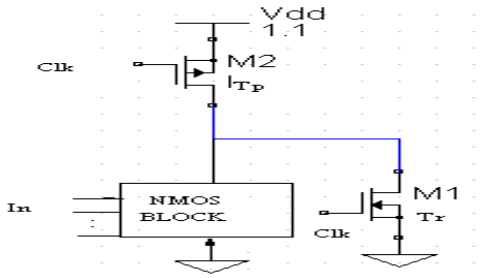

Fig 5: FTL structure.

This FTL consists of NMOS logic Block and two transistors (Tp-PMOS and Tr-NMOS). The multi input floating gate inverter by using FTL is as shown in Fig.6

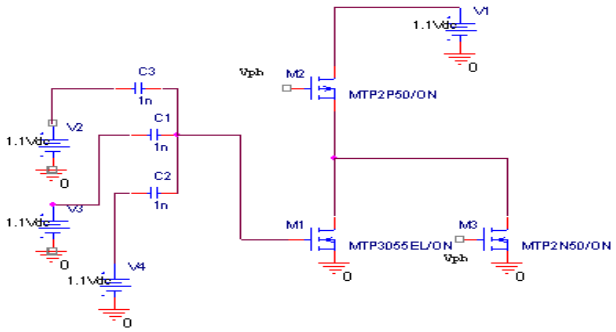

Fig 6: Multi input floating gate inverter by using FTL.

Unlike the dynamic logic families feed through logic rests the output nodes to low when the clock signal goes low, regardless of the input values, casaded gates firstly rise to their switching threshold value of Vth(typically about Vdd/2),performing a partial transition to a high gain point. at this point all gates in the circuit are in a high gain point. This feature distingue the FTL from other logic families. At Vth point any small variation in the input nodes would cause a fast variation of the voltage at the output node, and

as the cascade stages evaluation their inputs in a domino like fashion. The output nodes make only a partial transition from the Vth point to the high or low level. [1]Due to the reduction in both low to high and high to low propagation time delays, the FTL speed is high and is well suited to application where the critical path is made of a large cascade of inverting gates. Therefore the problems of non-inverting, charge redistribution and the need for output inverters are eliminated from the domino logics. In addition to this the principle of MIFG transistors, calculating weighted sum of all inputs at gate level and switching transistors ON or OFF depending upon calculated floating gate voltage greater than or less than switching threshold voltage, is utilized. The uniqueness of multi- input floating gate inverter lies in the fact that the switching voltage can be varied by selection of those capacitor values through which the inputs are coupled to the gate. Ordinarily, varying the Wp/Wn ratios of the inverter does the adjustment of threshold voltage. In multi- input floating gate inverter, varying the coupling capacitances to the gate can vary the switching point in DC transfer characteristics [7].

In order to design the full adder, the three input CMOS inverter has been taken since the carry is only the primary concerned for performance[8]. To get the carry the pull down transistor must be turned on (Vgs>Vth) if two out of three inputs are high. Then it is like majority not function. If equal capacitors are selected then according to the Basic equation

$$V_{fg} = K_1V_1 + K_2V_2 + K_3V_3 \qquad (4)$$

$$K_1 = \frac{C_1}{C_1 + C_2 + C_3} = \frac{C}{3C} = 0.33$$ Similarly K_2 and K_3 are also same. Here the Voltage is 1.1V so if only one of the input is high then Vfg(1.1*0.3=0.33) is less than threshold of the transistor So the pull down transistor is not "on".

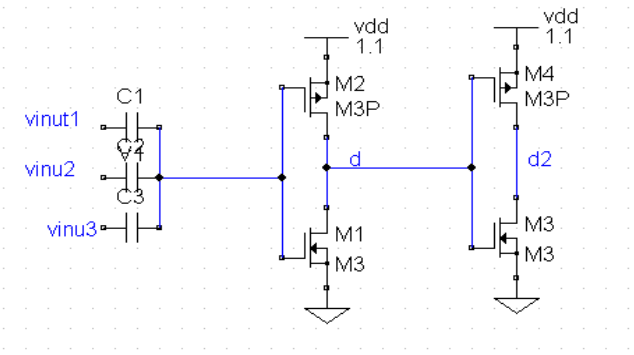

Fig 7 : Full adder carry generation.

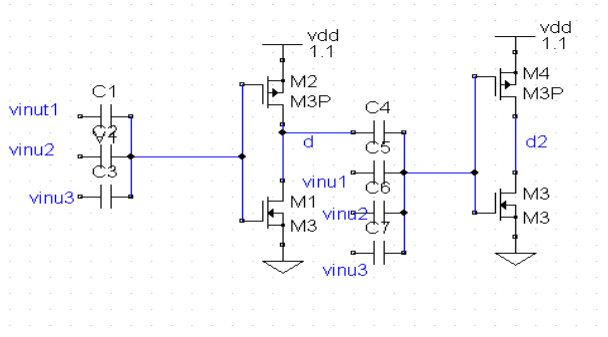

Fig 7(a): Full adder carry generation at second stage.

4.2 Carry look ahead adder: 2nd stage

The main novelty of this work is no requirement of propagation and generation signals. The inputs to the first stage of the inverter are a_0, b_0, c_0, a_1, b_1.Where a_0, b_0, c_0 are the first stage inputs and a1, and b1 are second stage inputs. The reduction of number of transistors is possible only through the understanding of the five input truth table. There are basically two observations from the table. One is whenever a1,b1 both are one then irrespective of the first stage three will be carry. Second one whenever there is carry from the first stage immediately that will affect the second stage. So considering all these into account C_1, C_2, C_3, C_4, C_5 values are decided in such a way that it satisfies the following condition.

$$\frac{C_1}{C_1 + C_2 + C_3 + C_4 + C_5} = 0.08$$

$$\frac{C_2}{C_1 + C_2 + C_3 + C_4 + C_5} = 0.08$$

$$\frac{C_3}{C_1 + C_2 + C_3 + C_4 + C_5} = 0.08$$

$$\frac{C_4}{C_1 + C_2 + C_3 + C_4 + C_5} = 0.38$$

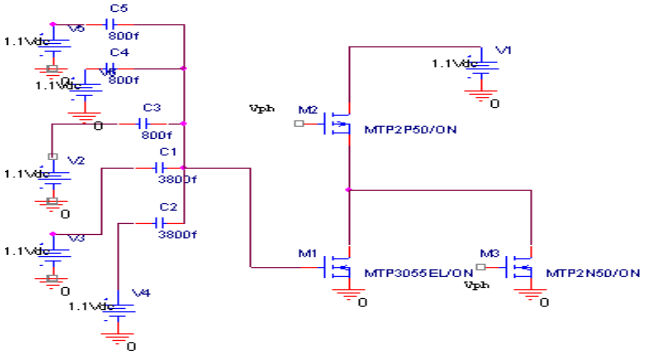

Fig 8: Carry look ahead adder (Two stages)

4.2.1 Full adder Sum:

First stage of the Ex-OR gate is same as that of CMOS carry. Here the second stage is the combination of input signals and fisrst stage carry output as shown in the below table.

Table 1. Truth table for first stage adder sum signal

A	B	C	Cfirststage	Sum
0	0	0	1	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

Sum is one when 1)Cout=1 and any of the inputs is one or 2)All there inputs are one. Accordingly capacitors are selected as shown in the below figure.

$$\emptyset_F = \frac{C1V1+C2V2+\cdots+CnVn}{Ctot} = \frac{\sum_{i=1}^{n} CiVi}{\sum_{i=n}^{n} Ci} \qquad (5)$$

Here n represents the number of inputs.V1, V2, …,Vn are the input signal voltages and C1, C2, …, Cn are the capacitive coupling coefficients between the floating gate and the substrate. The net potential on the floating gate is determined as a linear sum of all input signals weighted by the capacitive coupling coefficient [3]. The voltage signals are directly added at the gate level as shown in equation (5). Here the substrate potential and floating gate charge are neglected for simplicity. For the transistor to turn on, ΦF should exceed MOSFET threshold voltage, VTH and vice versa. Hence the weighted sum of all the inputs determines the "on" and "off" state of the MOSFET.

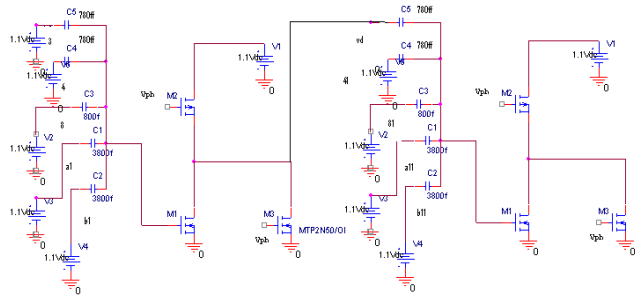

Fig 8 (a): Four stage carry circuit.

5. RESULTS

We have simulated and compare the power consumption and the performance of multiinput floating gate by using feed through logic carry generation to the multiinput floating gate carry alone. All the transistors that we have used have level 49 for their model. The net list of those circuits has been extracted and simulated using cadence (pspice tool). The power supply used here is 1.1v and capacitors are C_1=xx,C_2=xx,C_3=xx. From the Table 1, 2 it can be observed that the proposed multiinput floating gate carry by using Feed through logic has a less power consumption as well as delay when compared with normal multiinput floating gate without using FTL. The output waveforms for carry and sum signals are as shown blow Figures (10, 11, 12, 13, 14).

Table 2.comparison of power, delay and PDP for carry

Measurement	MIFG	FTL	4^{th} stage FTL Carry
Total Power	1.9E-06	1.22E-12	2.24E-12
Fall Time	965.95821p	49.4p	80,24P
Rise Time	27.897p	46.7p	558.23P

Table 3.comparison of power, delay and PDP for sum

Measurement	MIFG	FTL
Total Power	5.43E-06	2.42E-12
Fall Time	998.63464p	39.5p
Rise Time	327.197p	361.7p

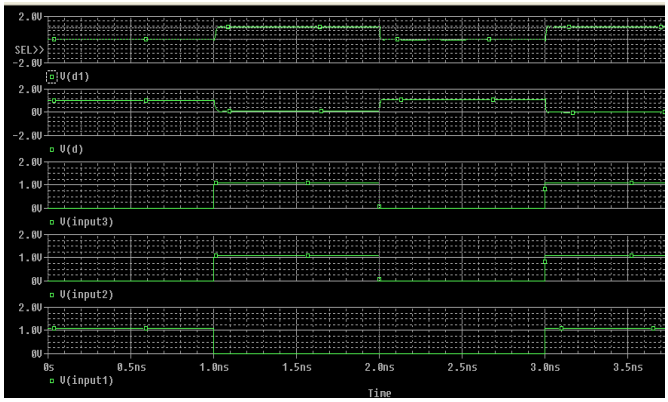

Fig 9: MIFG CMOS carry

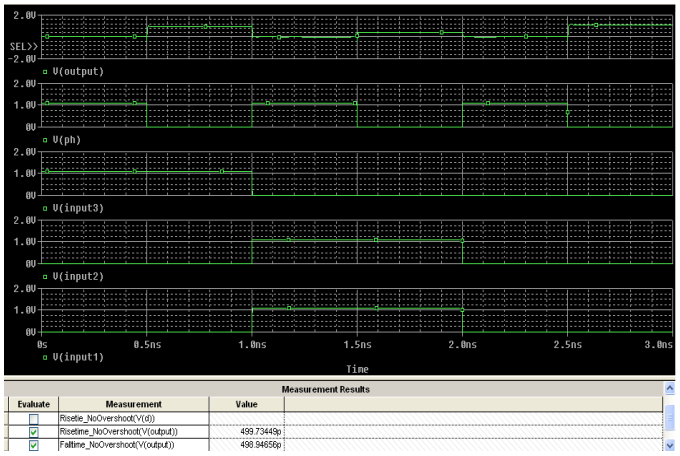

Fig 10: MIFG CMOS carry using FTL

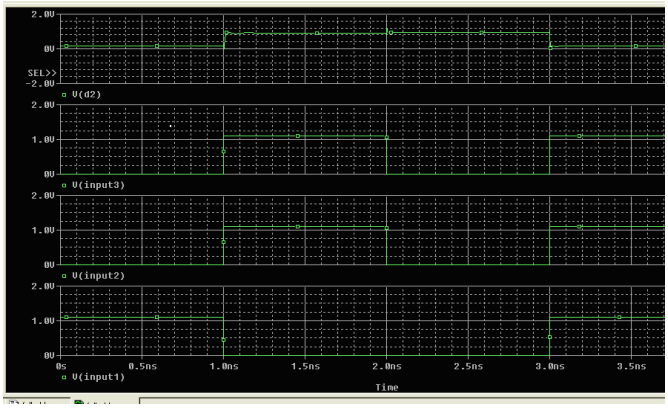

Fig 11: MIFG CMOS sum

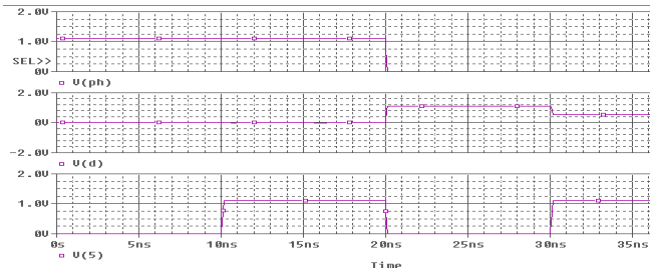

Fig 12: Transient analysis of simple FTL based inverter
Observed rise time is 6.9ps.Total power dissipation is 1.22E-12 W

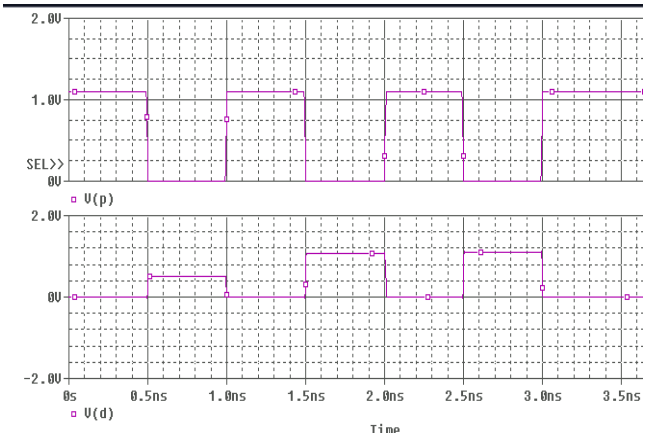

Fig 13: FT logic carry look ahead adder output(Vp)

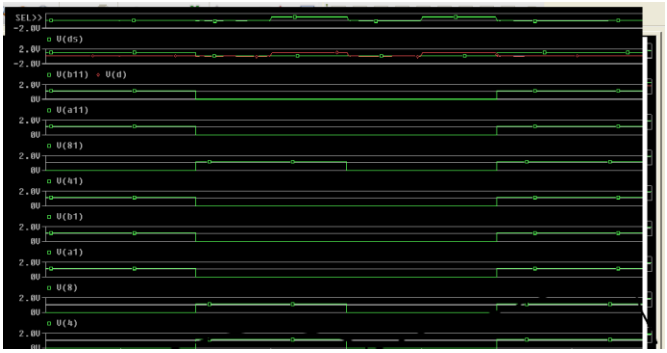

Fig 14: Fourth stage output wave forms

6. CONCLUTIONS

In this paper, a new multi input floating gate Carry look ahead full adder using feed through logic is implanted in nano technology. It is observed that the delay has been reduced to many fold (230-500ps), power as well and also area has been reduced. In case of cascading connection the number of transistors has been reduced to only 4 for each stage. It can be observed that if the number of stages is increase then the parasitic capacitance will increase and area will increase. Therefore the number of input capacitors are limited to two stage only.

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