Performance Analysis of FD-SOI MOSFET with Different Gate Spacer Dielectric

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ABSTRACT
As scaling down MOSFET devices degrade device performance in term of leakage current and short channel effects. To overcome the problem a newer device Silicon-on-Insulator (SOI) MOSFET has been introduced. The Fully Depleted (FD) SOI MOSFETs also suffer from short channel effects (SCE) in the sub 65 nm regime due to reduction in threshold voltage. Several investigations are going to reduce the SCE in FD-SOI MOSFET. This work is also facilitating for the improvement of performance of FD-SOI MOSFET using high-k gate spacer dielectric. The results from sentaurus TCAD simulator show that high-k spacer dielectric increases on state driving current and reduces off leakage current due to eminent vertical fringing electric field effect. This fringing field also lessens the SCE such as Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS). High-k spacer dielectrics ameliorate the I_{on}/I_{off}, transconductance and voltage gain of the FD-SOI MOSFET compare to the conventional oxide spacer.

General Terms
Drive current, Short channel effects (SCE).

Keywords
Silicon-on-Insulator (SOI), high-k spacer dielectric, fringing electric field, drain induced barrier lowering (DIBL), subthreshold slope (SS).

1. INTRODUCTION
Silicon technologies have progressed faster year to year. The main issue must be concentrate about silicon technologies is effects of reducing the dimension of devices. The scaling down of devices is strongly required to achieve high integration density and better device performance. Due to reduction in the channel length the short channel effects and leakage current become important issue that degrades the device performance [1]. To overcome the problem, a new circuit design techniques has been introduce for a newer technologies such as Silicon-on-Insulator (SOI). SOI refers to placing a thin layer of silicon on top of an insulator [2], usually silicon dioxide (SiO2) or known as buried oxide layer (BOX). Because of this BOX layer SOI MOSFETs provide less effect of scaling on performance parameters of device [3].

In order to increase reliability and reduce the leakage current, conventional offset gated or lightly doped drain structures have been widely used to reduce the lateral drain electric field [4]. However, these structures ineluctably decrease the ON driving current ION due to the extra series resistance. In mainstream CMOS technology, different offset spacer dielectrics are used to reduce the OFF leakage current I_{OFF} and improve the ON-state driving current I_{ON} [5]–[7]. The reduced series resistance effect due to an enhanced fringing field by using high-κ offset spacer contributes significantly toward the improvement of ON-state driving current I_{ON} to compete with other influences [4].

In this paper, the 25-nm node FD-SOI devices with three different spacer dielectrics are investigated using a 2-D device simulator Sentaurus [8], [9]. In section 2, we discuss about the short channel effects and leakage current in FD-SOI MOSFET. Device structure and simulation results are discussed respectively in section 3 and section 4. It is found that with the increase in spacer dielectric constant, the fringing field effect in the source/drain (S/D) extension region is enhanced, elevating the electron potential barrier of the channel film at the OFF, resulting in a reduced I_{OFF}. This also reduces the potential barrier and series resistance effect in the channel film at the ON-state, therefore increasing the ON state current I_{ON}. Also as we increase the spacer dielectric constant SCE i.e. subthreshold slope and DIBL improves. The results are also valid for bulk MOSFETs.

2. SHORT CHANNEL EFFECT IN FD-SOI
A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD}, x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise [10].

The short-channel effects are attributed to two physical phenomena:

1. The limitation imposed on electron drift characteristics in the channel
2. The modification of the threshold voltage due to the shortening channel length.

In this letter two short channel effects has been discussed and analyzed:

1. Subthreshold slope(SS)
2. Drain induced barrier lowering (DIBL)

2.1 Subthreshold Slope

It indicates how effectively the flow of drain current of a device can be stopped when V_{gs} is decreased below V_{th}. When Id-Vg curve of a device is steeper subthreshold slope will improve.

Subthreshold slope [11] is given by:

$$S_t = \left[\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right]^{-1} = \frac{kT}{q}\left(1+\frac{C_d}{C_i}\right) \quad (1)$$

Where C_d = depletion layer capacitance

C_i = gate oxide capacitance

A device characterized by steep subthreshold slope exhibits a faster transition between off (low current) and on (high current) states.

2.2 Drain Induced Barrier Lowering (DIBL)

In the weak inversion regime, there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. The barrier height for channel carriers should ideally be controlled by the gate voltage to maximize transconductance. The DIBL effect [12] occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, upon application of a high drain voltage. This increases the number of carriers injected into the channel from the source leading to an increased drain off-current. Thus, the drain current is controlled not only by the gate voltage, but also by the drain voltage.

For device modelling purposes, this parasitic effect can be accounted for by a threshold voltage reduction depending on the drain voltage [13].

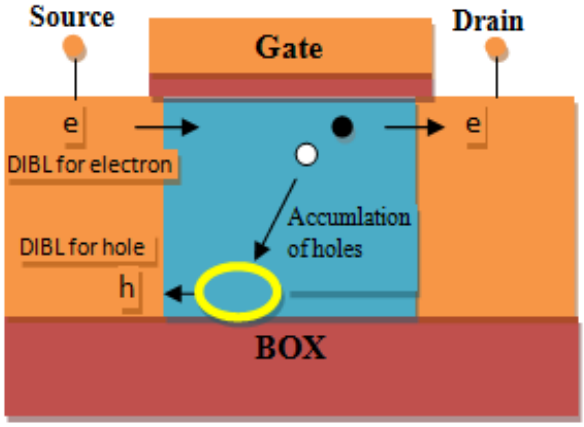

Fig 1: Three mechanisms determining SCE in SOI MOSFETs [14].

In addition to the surface DIBL, there are two unique features determining SCEs in thin-film SOI devices: 1) positive bias effect to the body due to the accumulation of holes generated by impact ionization near the drain and 2) the DIBL effect on the barrier height for holes at the edge of the source near the bottom of thin film, as illustrated in fig 1 [14].

3. TRANSPORT DESCRIPTION

The Sentaurus Device input file simulates the I_dV_g performance of an SOI NMOSFET device using the basic drift-diffusion transport model.

3.1 Drift diffusion model

The conduction in this model is governed by the Poisson's equation (2) and the equations of continuities of the carriers (3), (4). The Poisson's equation which couples the electrostatic potential V to the density of charge is given by

$$\nabla^2 V = \frac{-q}{\varepsilon}\left[p - n + N_D^+ + N_A^- + n_T\right] \quad (2)$$

Where n and p represent the densities of the electrons and the holes, respectively, N_D^+ and N_A^- are the ionized donor and acceptor impurity concentrations, respectively, n_T is the density of carriers due to the centre of recombination [15] and $\mathcal{E}$ is the dielectric constant. The transport equations express the current densities of the electrons and the holes; they are composed of two components, drift and diffusion [15].

$$\vec{J}_n = q\mu_n n\vec{E} + qD_n\vec{\nabla}_n \ , \quad (3)$$

$$\vec{J}_p = q\mu_q p - qD_p\vec{\nabla}_p \quad (4)$$

Where μ_n and μ_p are the electron and hole mobilities, D_n and D_p are the diffusion coefficients of electrons and holes and $\vec{\nabla}_n$ and $\vec{\nabla}_p$ are the two-dimensional gradients of concentration of electrons and holes. $\vec{E}$ is the electric field applied. The equations of continuities represent the carriers conservation in a volume element for the electrons and the holes, respectively.

$$\frac{\partial n}{\partial t} = GR_n + \frac{1}{q}\vec{\nabla}J_n \quad (5)$$

$$\frac{\partial p}{\partial t} = GR_p - \frac{1}{q}\vec{\nabla}J_p \quad (6)$$

The GR_n and GR_p terms describe the phenomena of recombination-generation and J_n and J_p are the current densities [15]. In a steady state regime, electro concentrations n, holes p, electrostatic potential V, and electrical current I are obtained from the solutions of equations (2)-(6) using the finite differences method. The solution of the equations consists of the discretization of the field in a finite number of points and the approach of the partial derivative, using finite differences method, in all the interior nodes of the field while taking in account the boundary conditions in order to obtain a linear system of equations in the following matrix form:

$$[M].[X] = [b] \ ,$$

Where M is the total matrix and b is the vector source.

To solve this system, we use the iterative method of Gausse-Seidel. It is particularly well adapted to the matrices of this type because they do not require additional storage and also present a good numerical convergence.

4. DEVICE STRUCTURE

To study the spacer dielectric effect on SOI MOSFET a schematic cross-sectional view of the SOI MOSFET is simulated using 2-D Sentaurus TCAD device simulator [8] is shown in fig 2. We assumed light channel doping concentration (1×10-17 cm-3) to avoid degrading of carrier mobility and more V_t variations. The doping concentration of S/D region is kept at $1\times10^{-19}cm^{-3}$. Gate length of the device that had been concentrated is 25nm. Silicon film thickness, gate oxide (SiO2) thickness and BOX thickness are 6nm, 0.6nm and 20nm respectively. We assumed n channel device and simulated the device for 4.40eV work function of metal gates of SOI MOSFET. Three offset spacer of different dielectric values were used, including SiO_2 (k=3.9), Si_3N_4 (k=7), HfO_2 (k=25) to study fringing field effect on the device performance.

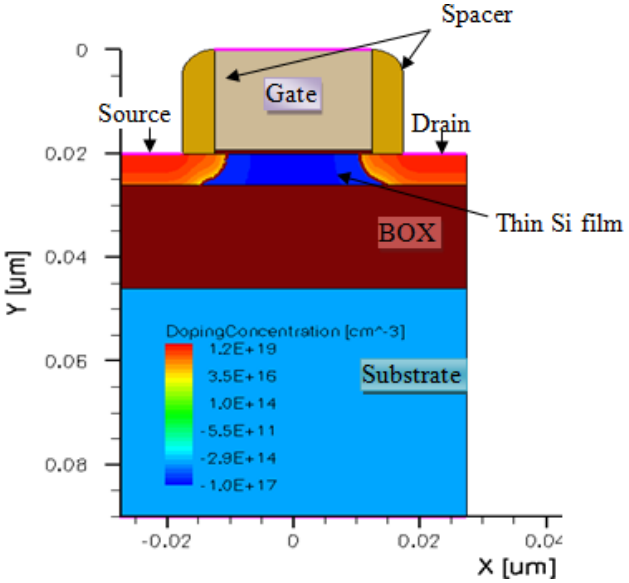

Fig 2: Illustration of simulated structure of FD-SOI NMOSFET.

5. SIMULATION RESULTS AND DISCUSSIONS

In this section different performance parameter of FD-SOI MOSFET for different gate spacer dielectrics has been discussed. Drift diffusion model has been used for extracting different parameters.

5.1 Drive Current (ON-state current) I_{ON}:

From simulation results fig 3 shows the vertical electric field along the channel direction for different spacer dielectric in ON-state condition (V_{gs}=V_{ds}=0.84v). The gate potential elevates the drain-side potential via offset sidewall spacers to reduce the electron barrier height in the thin film and also decreases the S/D series resistance in the extension regions (i.e., the junctions become more accumulated), resulting in an increased driving current I_{ON}. It also seen from fig 3 that high-k offset spacer provides better fringing field in extension region.

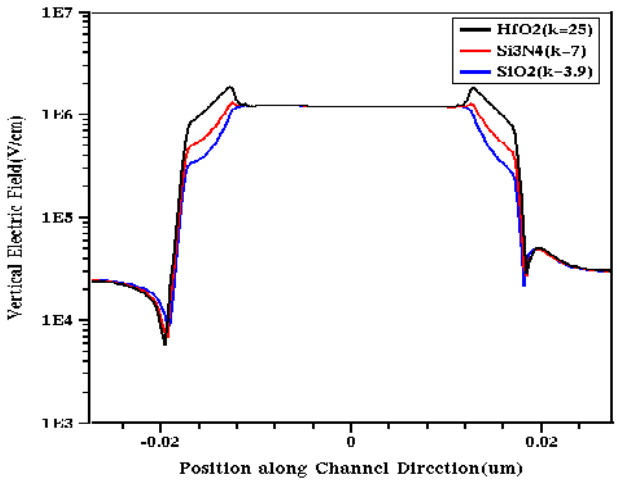

Fig 3: Vertical channel electric field with different offset spacer dielectrics at ON-state (V_{gs} = 0.84 V, V_{ds} = 084 V).

5.2 Transconductance g_m:

It measures the drain current variation with a gate-source voltage variation while keeping the drain-source voltage constant and is of crucial importance because it decides the ability of the device to drive a load. The transconductance has a important role in determining the switching speed of a circuit and voltage gain of MOSFET amplifiers. High transconductance devices yield circuits capable of high speed operation.

Fig 4 shows the drain current as a function of gate voltage for different spacer dielectric constant. This curve actually indicates the transconductance of SOI MOSFETs. As MOSFET size is reduced, the fields in the channel increase and the dopant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance.

Transconductance of a MOSFET

$$g_m = \left.\frac{\Delta I_{ds}}{\Delta V_{gs}}\right|_{V_{ds}} \tag{7}$$

From equation (7) transconductance measured by the slope of I_{ds}-V_{gs} curve. When Id-Vg curve of a device is steeper it shows better transconductance. In fig.4 HfO_2 (k=25) of high dielectric value shows steeper I_{ds}-V_{gs} curve than Si_3N_4 (k=7) and SiO_2 (k=3.9). So it provides better transconductance.

Voltage gain of a MOSFET device

$$A_v = g_m R_D \tag{8}$$

From equation (8) high dielectric value spacer also provides high voltage gain.

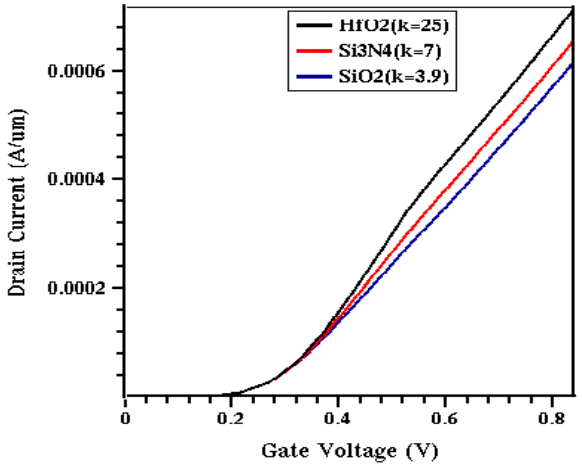

Fig 4: I_{ds}–V_{gs} characteristics of three dielectric offset spacer SOI devices. The transconductance increases with the κ value of the spacer.

5.3 Electron Concentration:

Fig 5 shows the electron concentration along the channel direction for different spacer dielectric. It shows that high-k dielectric provides higher electron concentration in extension region than conventional SiO_2 spacer, which further increase the ON-state current as describe above.

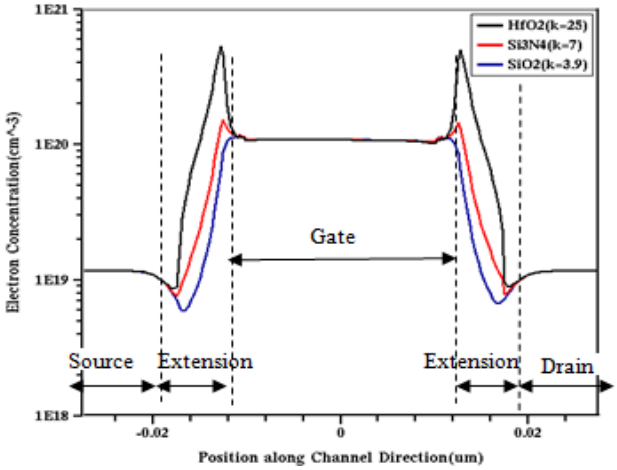

Fig 5: Electron concentration for different dielectric spacer.

5.4 Output Conductance g_d:

It measures the drain current variation with a drain-source voltage variation while keeping the gate-source voltage constant. It is a vital parameter for a device because it decides the drive current of a device.

Output conductance of a MOSFET

$$g_d = \left.\frac{\Delta I_{ds}}{\Delta V_{ds}}\right|_{V_{gs}} \qquad (9)$$

Fig 6 shows the drain current as a function of drain voltage for different spacer dielectric constant. This curve clearly shows the improvement of the driving current I_{ON} with the increase of the offset spacer dielectric constant as described above.

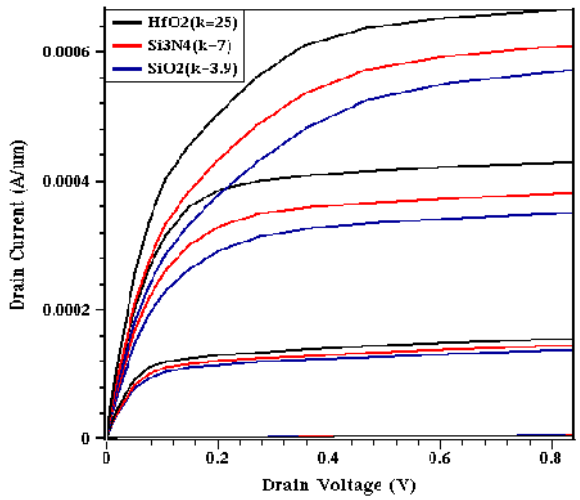

Fig 6: I_{ds}–V_{ds} characteristics of three dielectric spacer SOI devices. The driving current increases with the κ value of the spacer.

5.5 Leakage Current (OFF Current):

The electric field comes to the gate from the drain extension region and goes to the source extension region from the gate at the OFF, i.e., V_{ds} = 0.84V and V_{gs} = 0V. This implies that the gate potential elevated the source-side potential and lowered the drain-side potential via offset sidewall spacers, resulting in an increased electron barrier height to reduce the OFF current.

From fig 7 we see that high dielectric value spacer produce high fringing field which help to produce low OFF current.

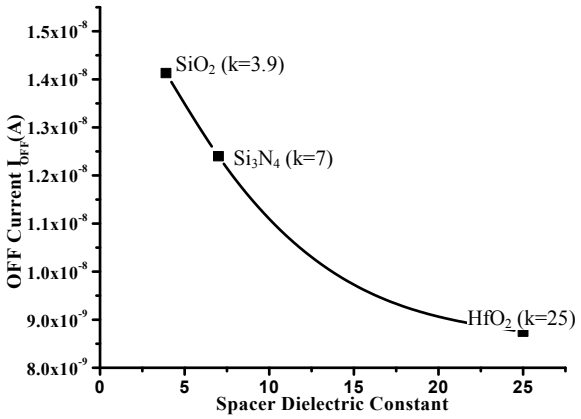

Fig 7: OFF-state current (V_{ds} = 0.84V and V_{gs} = 0V) for different spacer.

5.6 On Current OFF Current ratio(I_{ON}/I_{OFF}):

ON current to OFF current ratio is a vital performance parameter for SOI MOSFET Fig 8 shows the ON current to OFF current ratio for different spacer dielectric constant. As we increase the dielectric constant of spacer on state current increases and off state current decreases so I_{ON}/I_{OFF} increases and the device performance also increases. From figure 8 I_{ON}/I_{OFF} for HfO_2 is two twice than the conventional SiO_2 spacer.

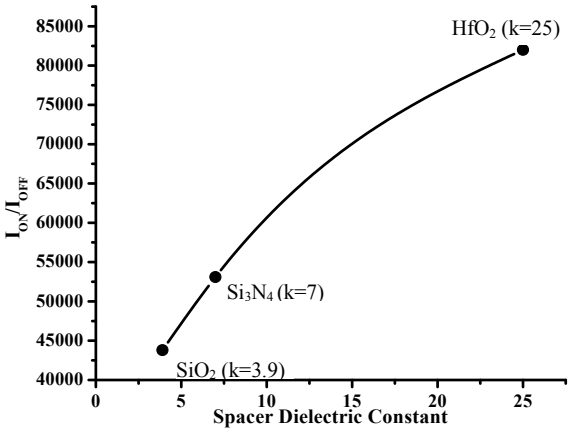

Fig 8: ON current to OFF current ratio for different spacer of different dielectric values.

5.7 Short Channel Effects:

Fig 9 shows the subthreshold swing characteristic for the 25-nm SOI device with different offset spacer dielectric constants. The subthreshold swing is improved as the offset spacer dielectric constant is increased. These results imply that the gate-to-channel control ability is enhanced due to the assistance of the high-κ offset spacer dielectric. As a result, a lower OFF leakage current and higher driving current 25-nm SOI devices can be achieved by using a high-κ offset spacer dielectric, thereby effectively reducing the power dissipation and increasing the performance of the transistor.

Fig 10 shows the variation in DIBL for different dielectric constant spacer. As the dielectric constant of spacer increases DIBL improves, this will further reduces the problem of threshold voltage roll-off. Reduced spacer-k value can effectively reduce drain coupling to the channel through the spacer and gate dielectric, thus reduce DIBL. A high-k spacer produce a higher out fringing electric field and provide better control over the junction depletion region near the drain side, as a result increase spacer-k value decreases DIBL.

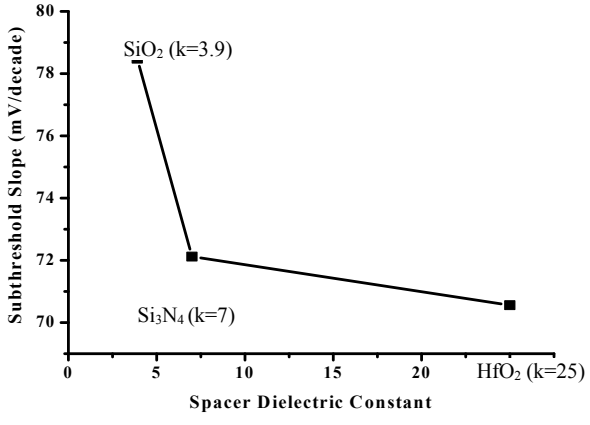

Fig 9: Subthreshold slope variation of an SOI device with different offset spacer dielectrics. It shows the excellent gate-to-channel control ability in the subthreshold region.

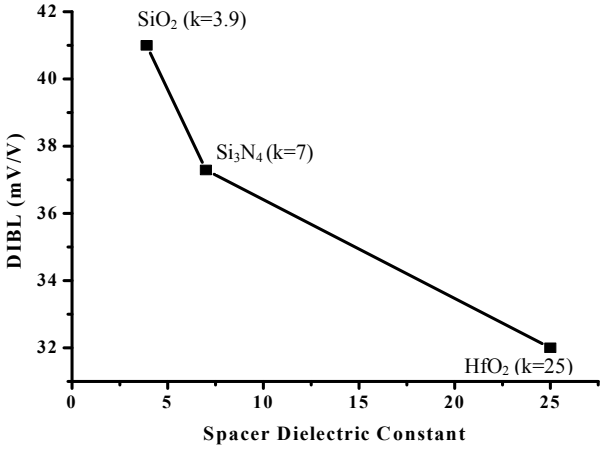

Fig 10: DIBL variation of an SOI device with different spacer dielectrics.

6. CONCLUSION

From Simulated results it can be conclude that spacer material with high dielectric values produces higher fringing field, which helps to reduce the barrier height between source and drain in on state resulting increses ON current (I_{ON}). ON current is 20% higher in case of HfO_2 (k=25) spacer than the conventional SiO_2 (k=3.9) spacer. In off state barrier height between source and drain is large for high-k spacer so it reduces OFF current 30% than the conventional SiO_2 (k=3.9) spacer. High-k spacer provides higher transconductance than conventional SiO_2 spacer. It also provides higher voltage gain, so we use SOI MOSFET devices with high-k spacer for amplification purpose. Also I_{ON}/I_{OFF} is higher in case of high-k spacer. High-k spacer improve short channel effects by imroving Subthreshold slope by 12% and reducing DIBL by 22% than conventional SiO_2 spacer. So high-k gate spacer is better option for coming SOI MOSFET devices.

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